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Low V_F 4H-SiC NiP Diodes Using Newly Developed Low Resistivity p-type Substrates

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Abstract

4H-SiC NiP diodes characteristics using newly developed low resistivity p-type substrates were demonstrated. The resistivity of the low resistivity p-type substrate is 1/3 of the conventional substrate. The forward voltage drop and the differential on-resistance of fabricated NiP diode with a 233µm thick n^- drift layer were 11.0V and 60.1mΩcm^2 at room temperature. To evaluate the forward voltage degradation, forward current stress tests were also performed. No stacking faults expansion was observed up to 1100A/cm^2 with utilization of a heavily doped p-type recombination enhancement layer on a p-type substrate.

1. Introduction

Ultra-high voltage 4H-SiC devices will be quite useful for Smart Grid components and high-voltage direct current (HVDC) transmission systems. Because they can downsize these systems and lose energy loss in comparison with Si devices. Up to now, several groups have reported SiC-IGBTs [1, 2, 3]. But in these reports, usually a p-type epitaxial layer was used as an injector layer. Although using p-type SiC substrates will make fabrication process of IGBTs conveniently, the conventional p-type SiC substrates were higher resistivity (over 2Ωcm) and crystal quality of them were much poorer than n-type SiC substrates. Thus, it is hard to use a p-type SiC substrate as an injector layer of the IGBTs. In this work, in order to apply a p-type substrate as an injector layer of the IGBTs in the future, we fabricated 4H-SiC NiP diodes using newly developed low resistivity p-type substrates [4] and demonstrate forward characteristics of them.

2. Device Structure and Fabrication Process

2.1 NiP diodes with a thin n^- drift layer

Fig.1 (a) shows the schematic cross-section of NiP diodes with a thin n^- drift layer. For comparison of the resistivity of p-type substrates, we also fabricated NiP diodes on a conventional p-type substrate. As a recombination enhancement layer, p^{++} buffer layers were grown on 4° off-axis heavily doped (>1e19cm^{-3}) 4H-SiC (0001) p-type substrates. The thickness and acceptor concentration of p^{++} buffer layers were 3.2µm and 7.5×10^{19}cm^{-3} for the low resistivity p-type substrate, 3.3µm and 2.7×10^{19}cm^{-3} for the conventional substrate. A 10µm thickness and donor concentration of 1.0×10^{16}cm^{-3} n^- drift layer was formed. To form the n^{++} and p^{++} contact layers, P atoms and Al atoms were implanted and activation annealing was performed. Doping density of P atoms and Al atoms were 3.0×10^{20}cm^{-3}.

2.2 NiP diodes with a thick n^- drift layer

Fig.1 (b) shows the schematic cross-section of NiP diodes with a thick n^- drift layer. On a 4° off-axis heavily doped (>1e19cm^{-3}) 4H-SiC (0001) p-type substrate with resistivity of 640 mΩcm at room temperature (1/3 of the conventional substrate), which result in resistance of 8.5 mΩcm^2 for a 133 µm thickness. After the p^{++} buffer layer and n^+ field stop layer were grown by chemical vapor deposition (CVD), a very thick 270µm n^- drift layer with donor concentration of 2.0×10^{14}cm^{-3} was formed. To obtain a low conduction loss with enough conductivity modulation, carrier lifetime enhancement process, carbon implantation and subsequent annealing process were used [5]. After annealing process, the implantation damage layer was removed by CMP. The thickness of remained n^- drift layer was about 233µm. As for the top contact layer, about 3.0µm thickness and donor concentration of 6.0×10^{18}cm^{-3} n^{++} layer were formed. The height of mesa was approximately 4.0µm. The effective carrier lifetime before device process measured by microwave photoconductivity decay (µ-PCD) increased to 14.7µs at room temperature, and 23.9µs at 250 ℃, respectively.

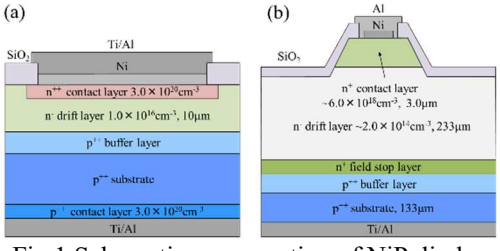

Fig.1 Schematic cross-section of NiP diodes. (a) with a thin n^- drift layer (b) with a thick n^- drift layer.

3. Results and Discussion

3.1 Comparison of the characteristics of NiP diodes with a thin n⁻ drift layer

Fig.2 shows the forward I-V characteristics of NiP diodes with a thin n⁻ drift layer at room temperature. The forward voltage drop and the differential on-resistance at 100A/cm^2 were 5.2V and 23.1mΩcm^2 for the low resistivity substrate and 9.8V and 64.8mΩcm^2 for the conventional substrate. The difference of the differential on-resistance between the low resistivity substrate and the conventional substrate were about three times. It approximately agreed with the difference of resistivity of the substrate.

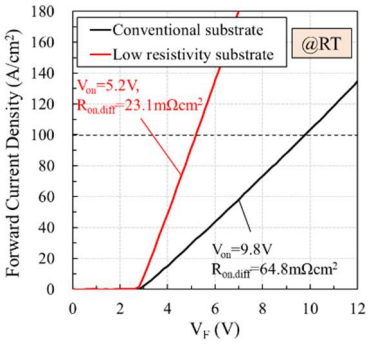

Fig.2 Forward characteristics of NiP diodes with a thin n⁻ drift layer at room temperature.

Fig.3 (a) shows the typical forward characteristics of a fabricated NiP diode with a thick n⁻ drift layer at room temperature to 200 ℃. The forward voltage continuously drops as the temperature increases. The forward voltage drop and the differential on-resistance at 100 A/cm^2 were 11.0 V and 60.1 mΩcm^2 at room temperature to 6.9 V and 32.2 mΩcm^2 at 200 ℃ respectively. Fig.3 (b) shows temperature dependence of the forward voltage drop and the differential on-resistance of fabricated NiP diodes at 100 A/cm^2. Since carrier lifetime is 14.7 μs at room temperature, which is enough for conductivity modulation toward a 233 μm thick n⁻ drift layer. As the contact resistivity presumed no more than 1 mΩcm^2, these observed temperature dependence of the differential on-resistance is thought that the temperature dependence of the hole injection, which came from ionization rate of Al ions.

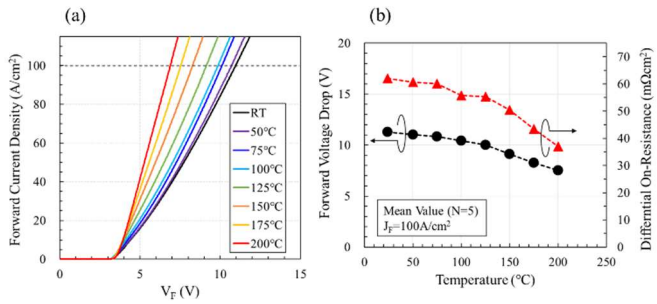

Fig.3 Forward characteristics of NiP diodes with a thick n⁻ drift layer at room temperature to 200 ℃.
(a) I-V characteristics of a NiP diode.
(b) Temperature dependence of the forward voltage drop and the differential on-resistance of NiP diodes.

3.2 Evaluation of the forward voltage degradation

Fig.4 (a) and (b) show EL images of a NiP diode with a thin n⁻ drift layer and a low resistivity substrate at the same region before and after forward current stress tests. The maximum forward current stress condition was 1100A/cm^2 at 150℃ for 10min. Up to 1100A/cm^2, no stacking fault expansion was observed. This means the p^{++} buffer layer effectively suppresses the electrons reaching to the substrate, where the basal plane dislocation which cause the expansion of stacking faults.

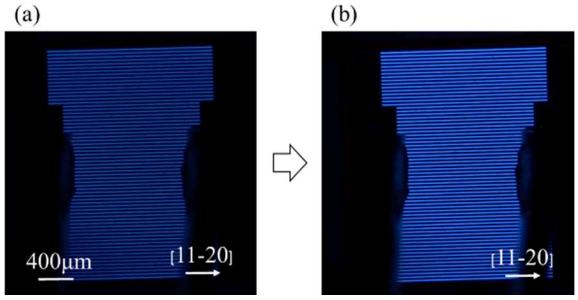

Fig.4 EL images of a NiP diode with a thin n⁻ drift layer and a low resistivity substrate.
(a) before (b) after forward current stress 1100A/cm^2 at 150℃ for 10min.

4. Conclusions

4H-SiC NiP diodes characteristics using newly developed low resistivity p-type substrates were demonstrated. The resistivity of the low resistivity p-type substrate is 1/3 of the conventional substrate. The forward voltage drop and the differential on-resistance of fabricated NiP diode with a 233μm thick n$^-$ drift layer at 100 A/cm^2 were 11.0 V and 60.1 mΩcm^2 at room temperature to 6.9 V and 32.2 mΩcm^2 at 200 ℃ respectively. To evaluate the forward voltage degradation, forward current stress tests were also performed. No stacking faults expansion was observed up to 1100A/cm^2 with a heavily doped p-type buffer layer on a p-type substrate. By optimizing p^{++} buffer layers, we could have a prospect to suppress forward voltage degradation when we apply a p-type substrate as an injector layer of SiC-IGBTs.

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