Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp515-516

3D SoC Design with TSV-less Power Supply Employing Highly Doped Silicon Via

Kota Shiba, Mototsugu Hamada, and Tadahiro Kuroda

Keio University
3-14-1 Hiyoshi, Kohoku-ku, Yokohama 223-8522, Japan
Phone: +81-45-566-1432 E-mail: shiba@kuroda.elec.keio.ac.jp

Abstract

A low cost power supply technique for 3D SoC is experimentally confirmed by using highly doped silicon vias (HDSV). A 100um x 100um HDSV in 2um-thick silicon wafer exhibits a resistance of 2.7Ω after wafer thinning, bonding, and annealing. A 9-stack 3D SoC is designed with HDSV power supply and its area overhead is calculated as 11%. Moreover, TCAD simulations show that the resistance of the same HDSV could be as low as 22mΩ, which turns into an area overhead of 0.09%.

1. Introduction

3D integration plays a key role while the conventional 2D scaling faces many red brick walls. Although many die stacking approaches rely on Through-Silicon Via (TSV), it requires additional wafer logistics and is costly. As for data communications between 3D-stacked chips, ThruChip Interface, which uses inductive coupling, was developed [1]. However, power was still delivered by TSV in a 3D SoC [2] where a room for cost reduction still remains.

Highly Doped Silicon Via (HDSV), a new way for power delivery with a deeper than normal and more highly doped well, can replace TSV [1]. In this paper, a proof-of-concept prototyping is shown with HDSV, and a 9-stack 3D SoC is designed with HDSV, where HDSV and TCI are used for and power delivery and data communications, respectively, as shown in Fig. 1.

2. Highly Doped Silicon Via

Fig. 2 shows a Wafer-on-Wafer (WoW) 3D integration process with HDSV. Highly doped regions for power vias are first created by implants, followed by nominal process for transistors and wires, and metal caps are added on the HDSV. Wafer is then thinned to a couple of microns. The HDSV on one die and the electrodes on the next die are connected by pressure using a room-temperature wafer bonding machine to create larger stacks.

Two types of impurities are possible to implement HDSV, P-HDSV and N-HDSV. P-HDSV is a highly doped p-well surrounded by normal n-well to isolate the p-well from p-substrate.

The test structure for electrical characteristics of HDSV is depicted in Fig. 3. In this work, an upper wafer with HDSV and a lower wafer with metal plugs and wirings are fabricated and connected with the same process shown in Fig. 2. Note that, with this structure, the obtained IV curve reflects the resistance of a pad–HDSV–wiring–HDSV–pad path.

Table I compares HDSV with TSV. While TSV needs an additional costly process and a new wafer logistics to form through electrodes, HDSV requires only implantation and annealing process in the same fab, which leads to cost reduction. Though the resistance of HDSV is higher than that of TSV, it is still low enough as will be discussed in Section 3 & 4.

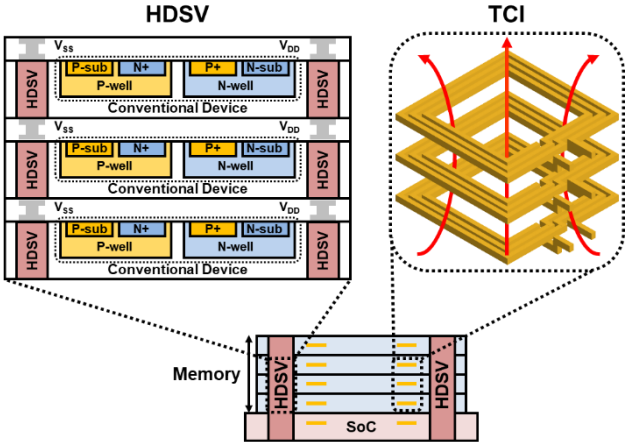

Fig. 1 3D system integration with HDSV and TCI.

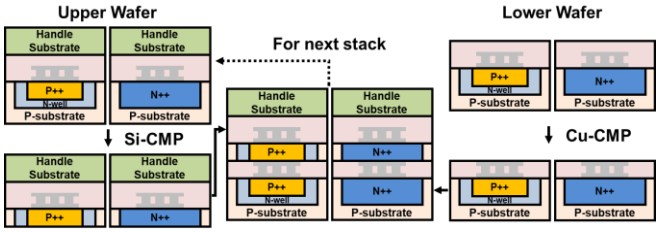

Fig. 2 Manufacturing process of HDSV.

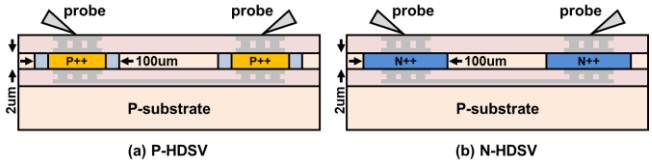

Fig. 3 Test stacked wafer of (a) P-HDSV and (b) N-HDSV.

3. Experimental Results with TCAD Simulations

Fig. 4 shows impurity concentration of P-HDSV (boron and phosphorus) and N-HDSV (phosphorus) by TCAD simulation. Diffusion time and temperature are 2 hours at 1200 ºC for boron and 4 hours at 1200 ºC for phosphorus in P-HDSV, and 4 hours at 1200 ºC for phosphorus in N-HDSV. The resistance of a 100 x 100um P-HDSV and N-HDSV is calculated as 16mΩ and 22mΩ, respectively, when the silicon wafer thickness is 2um.

Micro roughness of the upper wafer surface after Chemical Mechanical Polishing (CMP) is compared against impurity types in Fig. 5. In P-HDSV, there are 90nm-high steps

Table I Comparison table of TSV and HDSV

	TSV	HDSV
Wafer Technology	Etch and Via Fill	Implant and Anneal
Wafer Logistics	New model needed	Conventional model
Additional Cost	> 40%	A few %
Order of Resistivity	10 nΩm	10 – 100 μΩm

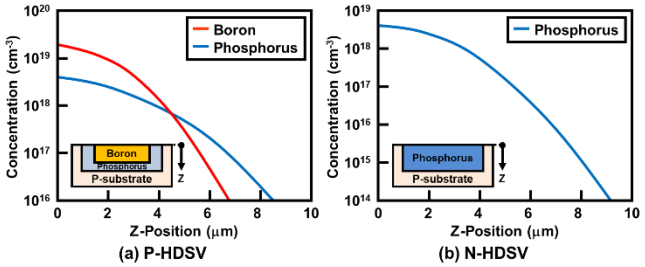

Fig. 4 Impurity concentration of (a) P-HDSV and (b) N-HDSV.

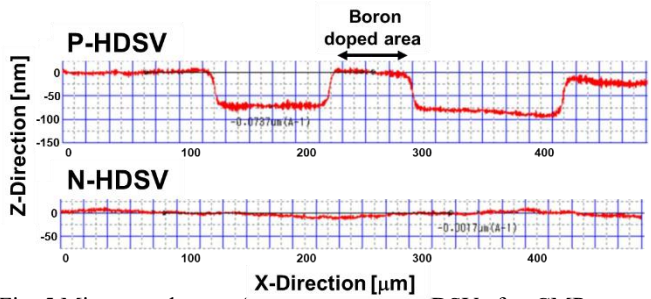

Fig. 5 Micro roughness of P-HDSV and N-HDSV after CMP.

between boron-dosed regions and the others. These steps come from the retardation of removal rate of CMP in highly boron-dosed cases [3]. The surface of N-HDSV after CMP is smooth enough for wafer bonding.

After wafer bonding, IV characteristics of HDSV are measured with the test structure shown in Fig. 3. The results are shown in Fig. 6.

P-HDSV exhibits non-ohmic characteristics. The resistance at 1.0V is about 300 Ω. N-HDSV exhibits better performance with a resistance of 30 Ω at 1.0V. After annealing, an ohmic contact is obtained and the resistance is reduced to 5.4 Ω as shown in Fig. 6(b), owing to the silicidation at Cu-Si interface.

However, the resistance is still considerably higher than one predicted by TCAD simulations.

Based on the micro roughness and the electrical characteristics described above, N-HDSV is better than P-HDSV. In the following section, 3D SoC design with N-HDSV will be discussed, where resistance of a 100um x 100um N-HDSV is assumed to be 2.7 Ω since the current in the test structure flows through two N-HDSVs.

In this scenario, N-HDSV is used for both VDD connections and GND connections. Though GND-biased n-well is not familiar in logic designs, we can find such designs in analog IC products. It means that latch-up issues in GND-biased n-well is manageable by design at the product level.

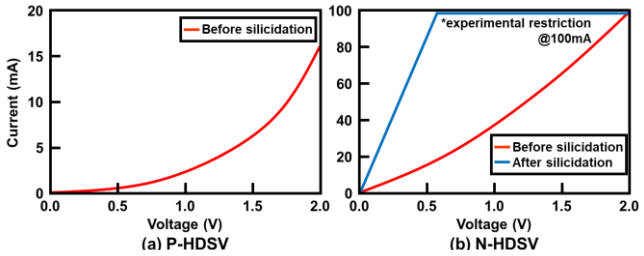

Fig. 6 Current-voltage characteristics of (a) P-HDSV and (b) N-HDSV.

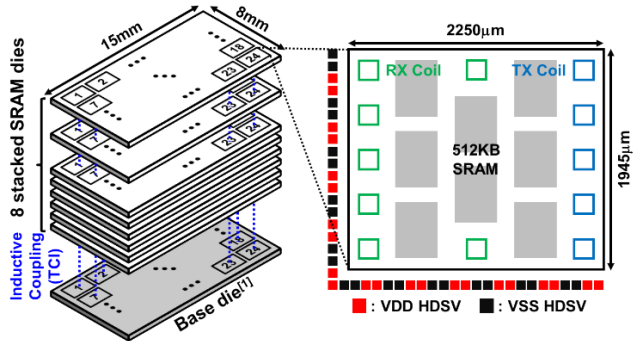

Fig. 7 Floorplan of 3D SRAM Module.

4. 3D SoC Design

A 3D SoC is designed by using N-HDSV power supply. The 3D SoC consists of one base die and 8 stacked SRAM dies. Data communications between the base die and 8 SRAM dies are done by TCI. Each SRAM die consists of 24 vaults working in parallel. Fig. 7 shows the floorplan of a vault of the SRAM die. The original design is fabricated in a 40nm CMOS technology and powered by TSV [2]. N-HDSV replace the TSV for power supply in this paper.

The maximum current consumption of a vault is estimated 50mA and IR drop by power lines is specified to be less than 50mV. Considering 8-series connection of SRAM dies, the resistance of HDSVs in parallel has to be less than 125mΩ.

Considering that the resistance of an N-HDSV is 2.7 Ω, it is calculated that 22 HDSVs for VDD and 22 HDSVs for VSS are required per vault. Supposing that the pitch of 100um x 100um HDSVs is 108um, area overhead for HDSV power supply is estimated to be 11%. When HDSV process is optimized and the resistance predicted by TCAD is obtained, which is 22mΩ per HDSV, the area overhead can be reduced as low as 0.09%.

5. Conclusions

HDSV is a promising technique for power supply of 3D SoC in combination with TCI data communications. It is experimentally shown that ohmic contact is obtained after wafer bonding. A 3D SoC is designed with N-HDSV and its area overhead is shown as 11%.

References

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