Differential Signal Balancer Embedded in Metal Wiring Layers of Silicon LSI

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Abstract

A new non-magnetic common mode filter embedded in metal wiring layers of silicon LSI was developed for ultra-high-speed differential transmission. Despite of thinner thicknesses for both metal and dielectric layers, its lumped circuit parameters are controlled well, and the obtained characteristics are almost comparable with that of the conventional ceramic laminated device.

1. Introduction

The signal data rate of the recent ultra-high-speed differential transmission technology such as USB 3.1 is already exceeding 10-Gb/s. To support such ultra-high-speed transmission, common mode filters (CMFs) such as the common mode choke (CMC) are employed to prevent the electromagnetic interference [1]. In recent, new principle CMC which are constructed without magnetic material to avoid the magnetic loss were developed [2]. However, miniaturizing it using thin film makes difficult to control the magnetic and capacitive stray coupling of the two inductors for differential transmission. [3].

The differential signal balancer (DSB) is also new CMF, which does not have an interline coupling. The DSB has superior characteristics; 1) absorbing noise in wide frequency range, 2) scattering the reflected noise in time domain, and 3) capability for the higher data rates up to 16-Gb/s [4]. Since DSB has been constructed using the multi-layer structure of low temperature co-fired ceramic (DSB-LTCC), its complex structure and the cost are obstacles to utilize the DSB to the wide range of applications.

To solve this problem, we have developed a DSB embedded in metal wiring layers (DSB-EIM) on a silicon LSI Chip. There is a report of realization a simple LC filter on semiconductor chip, however the common mode filter on chip has not been realized yet [5].

2. Design and Layout

Fig. 1 (a) and (b) show the equivalent circuits for the conventional DSB-LTCC and the developed DSB-EIM, respectively. Fig.1 (c) shows the detail of the delay line element (DL) that are used in both DSBs. The spiral inductor Ld and the capacitor Cd are the most important elements to construct the delay line. The stray coupling capacitance : Cb and magnetic coupling coefficient : k are formed between the electrodes of the stacked inductance Ld. The Cb and k are also important parameters that must be adjusted to construct the "all-pass filter type delay line". The parasitic metal resistances : Rs and Rc including via and/or contact resistances and the loss in capacitance must be controlled to

the value as small as possible. If any these parameters are not designed properly, the transmission characteristics will be greatly degraded.





In Fig. 1 (a) and (b), Ls is a small residual inductance to I/O. Lo and Rx are the spiral inductor and the meander resistor. Because of the length of spiral inductor and the width of meander shape layout, the parasitic resistance : Ro and the parasitic inductance : Lx are to exist with Lo and Rx, respectively. For the differential-mode signal, any Lo, Rx, Ro and Lx are not effective because these are connected to the differential balance point. On the other hand, for the common-mode noise, these components should be tuned carefully to attenuate the noise to return to circuit ground.

In order to obtain sufficient noise absorption effect in a wide frequency range, Rx and Lx are better to be connected in parallel like DSB-LTCC. However, in DSB-EIM, Ro and Rx are existing in a series. Therefore, the considerable efforts to optimize in the series connections of Lo-Ro and Lx-Rx were required.

Fig. 2 and 3 show the structures of conventional DSB-LTCC and developed DSB-EIM, respectively. The DSB-EIM is designed using the standard 180-nm CMOS process with 5 metal layers.





The dimensions for DSB-EIM are designed using electromagnetic (EM) simulator. Due to the limitation of the number of metal layers, the layout of DSB-EIM is spread in the plain direction. However, its area is a quite compact of 120- μ m × 250- μ m with the total thickness less than 10- μ m. The size was significantly reduced by two orders of magnitude in area ratio and reduced to about 1/6000 in volume ratio.

Fig. 4 (a) shows a photo of developed DSB-EIM in which the outer area of the DSB-EIM are surrounded with two differential signal pads (S) caught by three ground pads (G). The GSGSG probes with 40-GHz bandwidth are used for the measurement as shown in Fig. 4 (b). The characteristics of those pads and probes are to be canceled by the de-embed measurement technique.



3. Measurement result of DSB-EIM

The frequency responses of the equivalent circuit, EM simulation and an actual measurement are shown in Fig. 5.



Fig. 5 Frequency responses of DSB-EIM

The Sdd21 (differential-mode transmission) and the Scc21 (common-mode transmission) for the equivalent

circuit, the EM simulation and actual measurement show good agreement.

To confirm the availability of the noise reduction effect of DSBs, the pseudo random binary sequence (PRBS) responses for 10-Gb/s with 2.4-GHz Wi-Fi radio wave interferes and the skew of 20-ps at the signal source were analyzed by SPICE. Fig. 6 shows the receiving waveforms of 10-Gb/s PRBS signal at the end of the transmission line.





Fig. 6 (a) shows the case without DSB, the Wi-Fi radio wave interfere can be seen strongly. Fig. 6 (b) and (c) show the cases using conventional DSB-LTCC and using developed DSB-EIM, respectively. It is confirmed that the DSB-EIM can remove Wi-Fi radio wave interference sufficiently as well as the DSB-LTCC.

4. Conclusions

The DSB-EIM has been developed by embedding DSB into the metal wiring layers of LSI and its characteristics have been evaluated. The size was significantly reduced to about 1/6000 in volume ratio. We confirmed that the noise reduction effect of DSB-EIM is almost comparable to that of DSB-LTCC.

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