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Investigation of Gate-Length Dependence of Memory Window for 2D Ferroelectric-FET NVMs Considering the Impact of Spacers

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***Abstract*—In this work, within the static Preisach modeling framework, we investigate the impact of gate length scaling on the memory window (MW) of the ferroelectric-FET nonvolatile memory (NVM) with a 2D semiconducting transition-metal-dichalcogenide (TMD) channel (2D-FeFET) considering the fringing field through spacers. Our study indicates that, with spacers, the MW of the 2D-FeFET can be significantly improved with decreasing gate length (L_g) due to the enhanced internal gate charge at strong inversion and accumulation to polarize the ferroelectric. In other words, the spacer design in FeFETs may provide a way to compensate the MW reduction caused by the charge trapping effect in ultra-scaled FeFETs.**

I. Introduction

Thanks to recent discovery of ferroelectricity in crystalline orthorhombic-phase hafnium-oxide [1], the ferroelectric FET (FeFET) with CMOS compatibility and scalability has become a promising candidate for embedded nonvolatile memory (eNVM) [1]–[4]. To fulfill future high-density integration in NVM, 2D semiconducting TMDs such as MoS_2 [5]–[7] are very attractive channel material candidates to further extend the scaling of the FeFET memory, and the 2D-FeFETs (**Fig. 1**) with a monolayer MoS_2 channel have been demonstrated experimentally [8], [9]. However, the magnitude of the MW of ultra-scaled FeFETs is still restricted by the charge trapping effect [2]–[4]. With the scaling of L_g, how might the MW change for the 2D-FeFET considering the fringing field through the spacer has rarely been known and merits investigation.

In this work, with the aid of an analytical model capable of capturing the minor loop characteristic, the impacts of L_g scaling on the MW of 2D-FeFETs with various spacer materials are investigated.

II. Methodology

The model framework of the 2D-FeFET for write and read operations has been developed and shown in **Fig. 2**. To capture the minor loop behavior in a ferroelectric, the Preisach theory is adopted [10]. During the write operation, the magnitude of the hysteresis loop is determined by the pulse voltage (V_{Pulse}). The model is based on the concept of the electric field in the ferroelectric during the write operation, $E_{FE}(V_{Pulse})$, which can be determined by coupling the Preisach dipole polarization model [11] with the Q_{mos}-V_{mos} model of a 2D-FET [6], [7] for a given V_{Pulse}. With the solved $E_{FE}(V_{Pulse})$, during the read operation, the static Preisach P-E relationship [10], [11] can be self-consistently solved with the Q_{mos}-V_{mos} model of a 2D-FET again to obtain the drain current and polarization charge at each bias condition. In this work, HfZrO is used as the ferroelectric material with P_r = 20 μC/cm^2, P_s = 23 μC/cm^2, E_c = 1.5 MV/cm and $\varepsilon_{FE} = 30\varepsilon_0$ [12]. The fringing capacitance for the underlying 2D-FET with spacers is extracted via the TCAD simulation [13].

III. Results and Discussion

Fig. 3 shows that, compared with the intrinsic 2D-FeFET, the MW of the 2D-FeFET with spacers can be substantially increased with decreasing L_g, especially for the high-K spacer. The extraction of the MW is defined by $V_{T,\,erase} - V_{T,\,program}$ and the threshold voltage (V_T) is extracted based on the constant current method shown in the inset. The intersections of load lines of the underlying 2D-FETs with the Q_{FE}-V_{FE} hysteresis loop also show the larger MW for the short-channel 2D-FeFET with the SiO_2 spacer (see **Fig. 4**).

To explain this difference, **Fig. 5** shows the change of E_{FE} during the write operation with L_g scaling. It can be seen that, compared with the intrinsic 2D-FeFET with a nearly constant $E_{FE}(V_{Pulse})$, the $E_{FE}(V_{Pulse})$ of the 2D-FeFET with SiO_2 spacers increases with decreasing L_g. This difference results from the Q_{mos}-V_{mos} characteristics in **Figs. 6(a) and 6(b)**. Different from the intrinsic 2D-FeFET with merely a slight change of Q_{mos} in subthreshold region, the Q_{mos} of the 2D-FeFET with SiO_2 spacers increases both in strong inversion and accumulation regions with decreasing L_g (results from the fringing capacitance through spacers shown in **Fig. 6(d)**), which can offer more charges to polarize the ferroelectric during the write operation, thus enhancing the MW.

Fig. 5 also shows that the E_{FE} during programming is larger than that during erasing. This can be explained by the larger amount of electrons at strong inversion than the holes at accumulation for a given $|V_{mos}|$. Note that, a slightly increased $E_{FE}(V_{Pulse})$ during erasing for the intrinsic 2D-FeFET with decreasing L_g (see **Fig. 5**) stems from a slight increase of holes at accumulation (see **Fig. 6(a)**) due to the impact of intrinsic drain coupling on C_{mos} at subthreshold [7] (even though the C_{mos} in accumulation region remains constant in **Fig. 6(c)**). This slightly increased $E_{FE}(V_{Pulse})$ during erasing leads to a small increase of MW for the intrinsic 2D-FeFET with a short L_g in **Fig. 3**.

Although the MW of ultra-scaled FeFETs is still restricted and hard to be enlarged by increasing the write pulse voltage or width due to the charge trapping effect [2]–[4], the spacer design in FeFETs may provide another way to compensate for the loss of MW.

Acknowledgement

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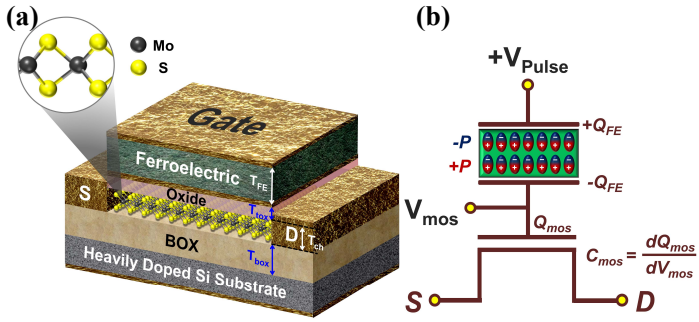

Fig. 1. **(a)** Schematic of the 2D-FeFET (T_{ch} ~ 0.65 nm) with T_{tox}, T_{box} and T_{FE} the interlayer oxide, buried oxide, and ferroelectric thicknesses, respectively. **(b)** Equivalent capacitor network of the 2D-FeFET with P the polarization charge, Q_{FE} the gate charge, Q_{mos} the internal gate charge, V_{Pulse} the pulse voltage, V_{mos} the internal gate voltage, and C_{mos} the internal gate capacitance.

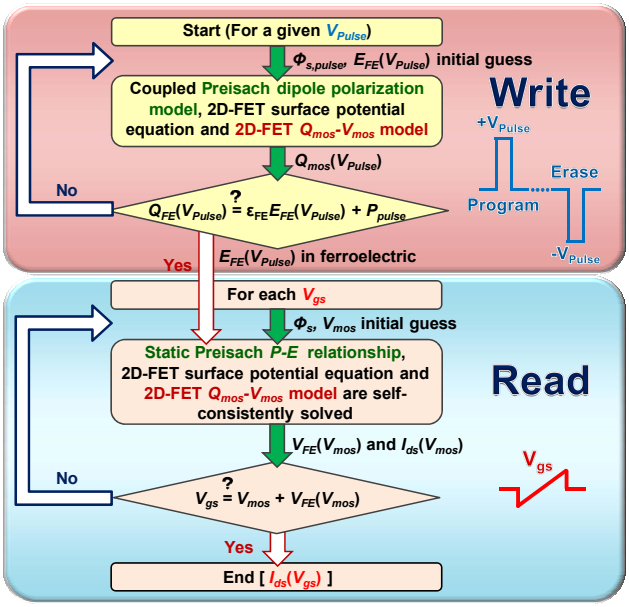

Fig. 2. Model framework of the 2D-FeFET for Write/Read operations. During Write operation, the magnitude of the hysteresis loop is determined by the V_{Pulse} [through $E_{FE}(V_{Pulse})$] and can be calculated by coupling the Preisach dipole polarization model with the Q_{mos}-V_{mos} model of the underlying 2D-FET. After Write operation, the I_{ds} can be obtained during Read operation.

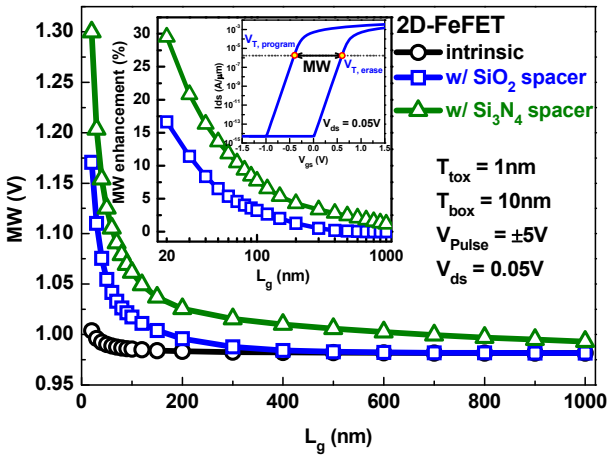

Fig. 3. The MW of the 2D-FeFET can be increased with decreasing gate length, especially for the 2D-FeFET with high-K spacers.

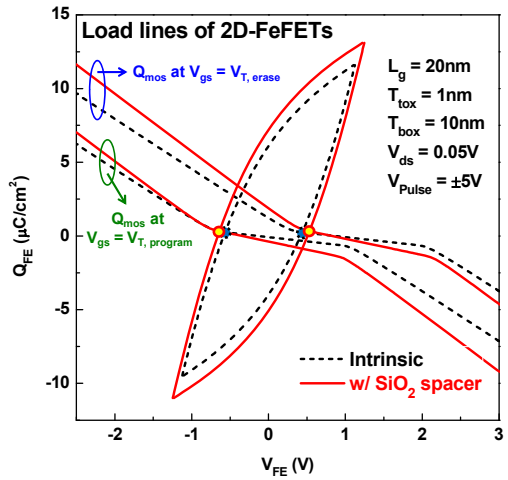

Fig. 4. The load lines of the underlying 2D-FETs intersect with the Q_{FE}-V_{FE} hysteresis loop at $V_{gs} = V_{T,\,erase}$ and $V_{T,\,program}$ for the intrinsic 2D-FeFET and the 2D-FeFET with SiO_2 spacer. V_{FE} is the voltage drop across the ferroelectric.

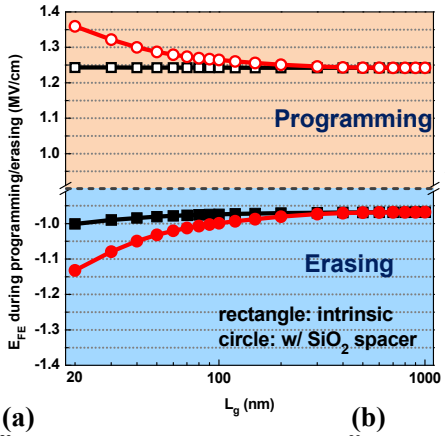

Fig. 5. Different from the intrinsic 2D-FeFET with an almost constant E_{FE} during Write operation, the E_{FE} of the 2D-FeFET with the SiO_2 spacer increases with decreasing L_g. This explains **Fig. 3**.

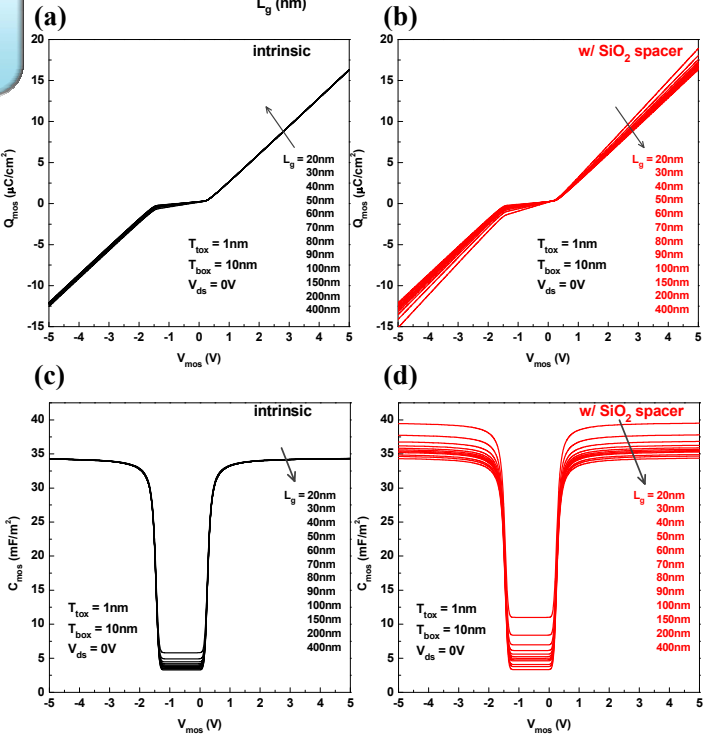

Fig. 6. The Q_{mos}-V_{mos} and C_{mos}-V_{mos} characteristics of the intrinsic 2D-FET [**(a)** and **(c)**] and the 2D-FET with SiO_2 spacers [**(b)** and **(d)**] showing the change of E_{FE} during Write operation with the L_g scaling in **Fig. 5**.