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A 65nm CMOS Process 4.2V Battery Charging Cascode SIDO Boost Converter with 87% Maximum Efficiency for RF Wireless Power Transfer Receiver

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Abstract

This paper presents a cascode single-inductor-dual-output (SIDO) boost converter fabricated in 65nm CMOS process for RF wireless power transfer (WPT) receiver. 2.5V I/O transistor cascode PFETs are used for 4.2V Li-ion battery output while 2.5V cascode NFETs are newly used for 1V output to supply low voltage internal control circuit. By using NFETs, 1V output with 5V tolerance can be achieved. Measurement results show conversion efficiency of 87% at P_{IN}=7mW.

1. Introduction

For Internet of Things (IoTs) applications, such as sensor network for industrial equipment in factory automation, RF WPT is attractive because power supply wiring to the sensors can be eliminated. Considering the distance from TX to the sensor (RX) of about 1~10m, 5.7GHz is chosen for RF [1]. Fig. 1 shows a simplified schematic diagram of the RF WPT system. To receive -10~15dBm range RF power in the RX power management circuit, 65nm CMOS process is chosen. Sub-100nm process is also favorable to reduce the power consumption of the control circuit since low voltage (1V) transistor is available. On the other hand, since a Li-ion battery is used for the output, 4.2V tolerance is required at the power stage of the boost converter. From these requirements, this paper proposes a SIDO boost converter that supplies 1V output to the internal control circuit and Li-ion battery compatible voltage output. Although the output voltage configuration is similar to [2], the proposed power stage does not use 5V thick oxide transistor but use cascode 2.5V I/O transistors.

2. Proposed Cascode SIDO Boost Converter Design

Fig. 2 shows the block diagram of the proposed boost converter which consists of the proposed cascode SIDO power stage, low power control circuit including clock generator (CLK generator) and V_{MID} regulator. The first output V_{OUT1} generates 1V power supply voltage for the control circuit and the second output V_{BAT} is connected to a Li-ion battery. Using 1V power supply contributes to low power consumption of the control circuit. For voltage regulation, clocked comparators are used instead of continuous-time comparators to reduce the quiescent current. Fig. 3(a) shows the detail of the cascode SIDO power stage and Figs. 3(b)-3(d) depict its operation states. By cascoding 2.5V I/O transistors, 5V tolerance is obtained where V_{MID}=1/2V_{BAT} is generated at V_{MID} regulator. It should be noted that the transistors connected to V_{OUT1} is 2.5V NFETs. If 2.5V PFETs are used, the gate voltage requires V_{BAT} to turn off when V_X node becomes V_{BAT} (up to 4.2V), which now exceeds the gate oxide voltage tolerance because V_{OUT1} is 1V. Also, the body of these NFETs are always connected to a lower potential by the low voltage selector to prevent unintended body diode conduction. Fig. 4 shows the V_{MID} regulator where V_{MID} is regulated between V_H and V_L (V_H-V_L is set to 50mV at V_{BAT}=4.2V) by turning on and off PMID or NMID transistors at a frequency of ϕ_{MID}.

Table 1 and Fig. 5 show SIDO control policy and waveforms, respectively. If V_{OUT1} is lower than the reference voltage, power is supplied to V_{OUT1} prior to V_{BAT} in order to ensure proper control operation. Fig. 6 shows the simple configuration and operation of CLK generator. The clocks provided to the clocked comparators are generated from low power 1.6MHz oscillator followed by logic circuits. To realize frequency-sweeping voltage monitor based on [3] for input regulation, ϕ_{IN} rising edge frequency is halved every cycle so that ϕ_{IN} becomes slower as V_{IN_DC} rise becomes slower when input DC power is low. The power consumption of the control circuits and power stage driver automatically reduces when the input power is low because the operation frequency goes down.

3. Measurement Results

The proposed boost converter is fabricated by 65nm CMOS process. Fig. 7 shows chip microphotograph and parameters of the external components. The die occupies an area of 1.1×1.1 mm^2. Fig. 8 shows the measured waveforms of the input voltage V_{IN_DC}, V_{BAT}, V_X, and ϕ_{IN}. It can be confirmed that the boost converter is operating properly. Fig. 9 plots the measured power conversion efficiency versus I_{LOAD} at V_{BAT}=4V. The maximum efficiency of the proposed boost converter is 87% at P_{IN}=7mW and I_{LOAD}=1.6mA. The total power consumption of the boost converter is 824μW at P_{IN} of 7mW and the power consumption of the 1V supply control circuit is 24μW. Table 2 shows a comparison with the recent boost converters that are aimed for energy harvesting.

4. Conclusion

This paper proposes a SIDO boost converter fabricated in 65nm CMOS process for RF WPT receiver. In order to meet the specifications for low power control, RF integration and high voltage output, the SIDO architecture and cascode power stage are proposed. The proposed circuit is successfully demonstrated and achieves 87% power conversion efficiency at measurement.

Acknowledgements

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References

[1] K. Murata et al., *IEEE EuMC*, pp. 170-173, 2018. [2] Y. Toyama et al., *IEEE A-SSCC*, pp. 9-12, 2016. [3] S. Y. Jung et al., *IEEE Symp. VLSI Circ.*, pp. 204-205, 2017. [4] P. H. Hsieh et al., *IEEE TCAS-I*, vol. 62, pp. 1528-1537, 2015. [5] A. Shrivastava et al., *IEEE JSSC*, vol. 50, pp. 1820-1832, 2015.

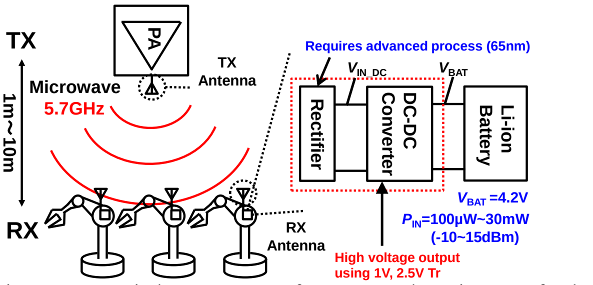


Fig. 1 Microwave RF wireless power transfer system and requirements for the DC-DC converter.

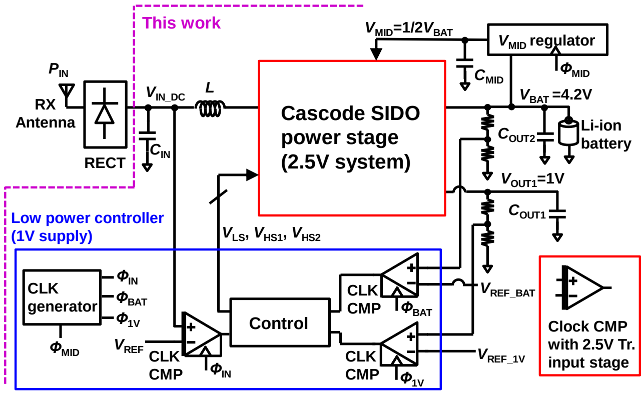


Fig. 2 Block diagram of the proposed circuit.

Table 1 State for SIDO control.

V_{OUT1}	V_{BAT}	Power provided to
>1V	>4.2V	Stop
<1V	>4.2V	V_{OUT1}
>1V	<4.2V	V_{BAT}
<1V	<4.2V	V_{OUT1}

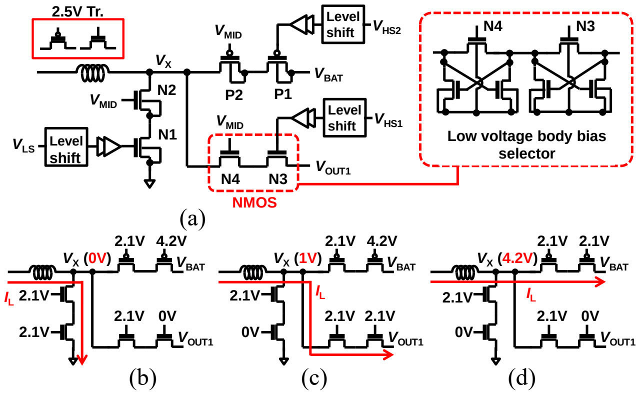


Fig. 3 (a) Schematic of the proposed cascode SIDO power stage, (b) N1 and N2 on state, (c) N3 and N4 on state, (d) P1 and P2 on state.

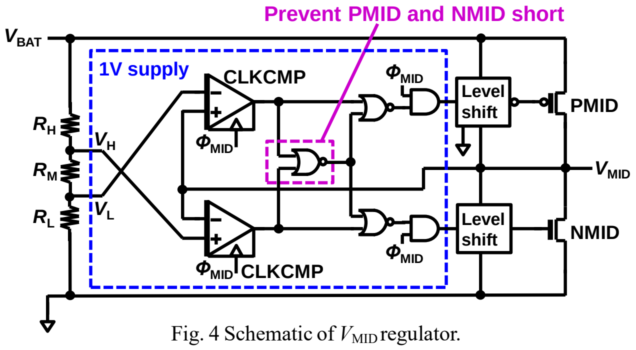


Fig. 4 Schematic of V_{MID} regulator.

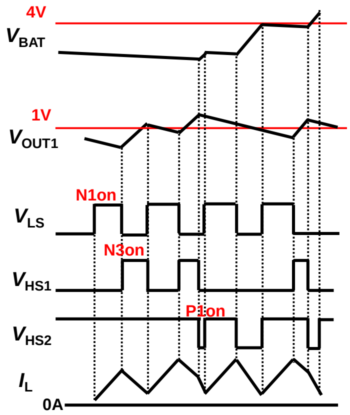
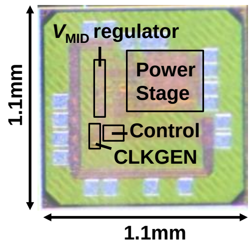


Fig. 5 Timing diagram of the SIDO control.



L	1mH
C_{IN}	10nF
C_{OUT1}	1μF
C_{OUT2}	1μF
C_{MID}	0.1μF

Fig. 7 Chip micrograph.

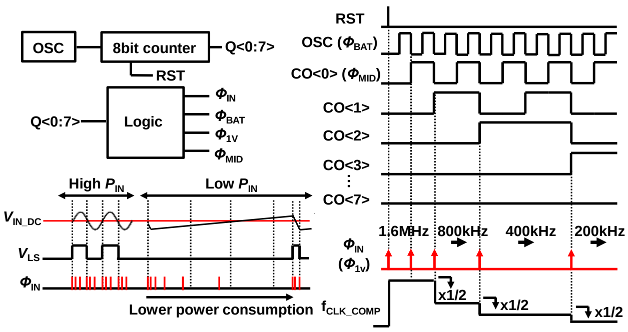


Fig. 6 Schematic and timing diagram of the frequency sweeping control.

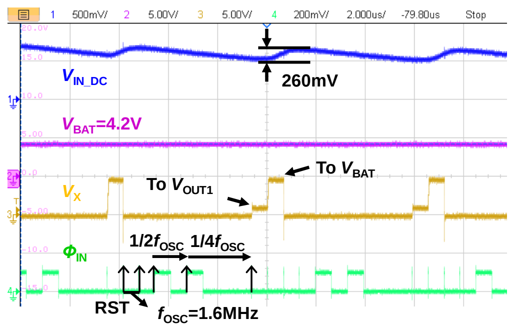


Fig. 8 Measured oscilloscope waveforms.

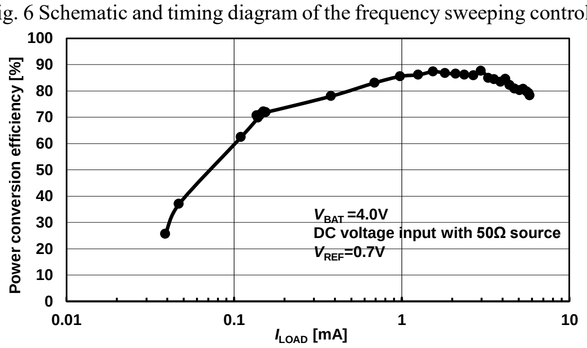


Fig. 9 Measured power conversion efficiency versus I_{LOAD}.

Table 2 Comparison with the recent works.

	This work	[2]	[3]	[4]	[5]
Applications	RF Wireless Power Transfer	Thermoelectric Energy Harvesting	Energy Harvesting	RF Energy Harvesting	Thermoelectric and Solar Energy Harvesting
Process	65nm	0.18μm	0.25μm	0.18μm	0.13μm
V_{OUT}	※2.6~5V	0~5V	2.5~4.1V	2V	1.1V
Input Power Range P_{IN}	30μW~30mW	-	20nW~140 mW@ V_{IN}=2V	-12dBm~	-
Maximum Efficiency	87%	69%@V_{IN}=100 mV	94%@V_{IN} =2V	35.7%(RECT +DCDC)	83%@V_{IN}=0.3V

※ V_{MID} externally supplied.