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A 42-mV Startup Ring Oscillator Using Self-Bias Inverters for Extremely Low Voltage Energy Harvesting

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Abstract

This paper presents a ring oscillator (ROSC) capable of operating at extremely low supply voltage. The proposed ROSC consists of gain-enhanced self-bias inverters. The voltage gain of the proposed inverter is improved by controlling body bias voltages. Measurements of a prototype chip demonstrated that our proposed ROSC can operate at extremely low supply voltage of 42 mV.

1. Introduction

Thermoelectric generators (TEGs) have attracted attention as an alternative energy source because they can generate energy from a subtle temperature difference. However, the output voltage of the TEG is too low to operate application circuits and systems. To address this issue, DC-DC converters are widely used to generate a sufficient higher voltage. As a first step to realize such converters, an extremely low voltage oscillator is required.

A ring oscillator (ROSC) consisting of inverters is widely used because it can operate at lower supply voltage. However, the voltage gain of the CMOS inverter decreases as the supply voltage decreases, and thus it is quite difficult to operate at sub-100mV supply voltage, which is a typical output voltage range of the TEG with a small temperature difference.

In this paper, we propose an ROSC capable of operating at extremely low supply voltage. Our ROSC consists of gain-enhanced self-bias inverters. The voltage gain of the proposed inverter is improved by controlling body bias voltages. Measurements of a prototype chip demonstrated that the proposed ROSC can operate at extremely low voltage of 42 mV.

2. Proposed Gain-Enhanced Inverter

Figure 1 shows a schematic of the ROSC. An odd number of inverters are connected in series and the output node is fed back to the first-stage input node. For oscillation to begin, the voltage gain must be greater than unity.

Figure 2 shows a schematic of a CMOS inverter and illustration of the voltage transfer curve (VTC) at low supply voltage V_{DD} (e.g., V_{DD} is lower than threshold voltage V_{TH} of MOSFET). When current of nMOSFET I_N is equal to that of pMOSFET I_P, the voltage gain of the inverter ($|A_{INV}|_{MAX}$) becomes maximum and can be calculated as

$$|A_{\mathrm{INV}}|_{\mathrm{MAX}} = \left\{ e^{\left(\frac{V_{\mathrm{DD}}}{2V_{\mathrm{T}}}\right)} - 1 \right\} / \eta, \qquad (1)$$

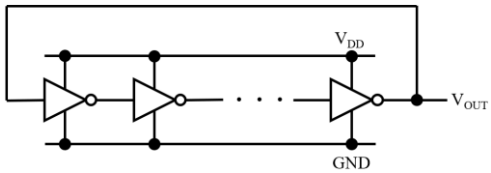

Fig. 1 Schematic of the ring oscillator (ROSC).

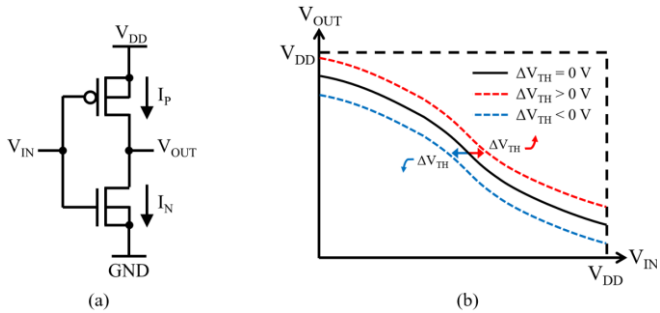

Fig. 2 (a) Schematic of the CMOS inverter and (b) voltage transfer curve with ΔV_{TH} as a parameter.

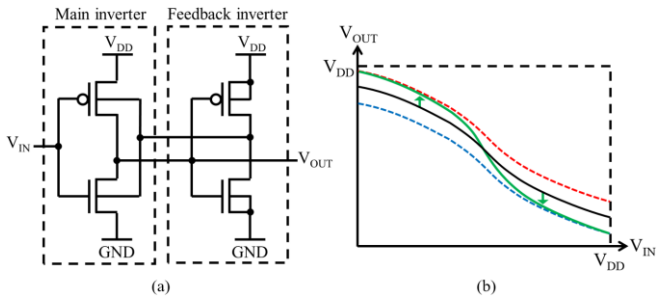

Fig. 3 (a) Schematic of the proposed self-bias inverter and (b) voltage transfer curve.

where η is the subthreshold slope factor and V_T is the thermal voltage. As shown in Eq. (1), the voltage gain decreases as V_{DD} decreases.

The VTC strongly depends on the threshold voltage difference ΔV_{TH} between nMOS and pMOSFET ($\Delta V_{TH} = V_{TH,N} - |V_{TH,P}|$). Therefore, as shown in Fig. 2(b), the VTC shifts according to the value of ΔV_{TH}. We consider using this characteristic to improve the voltage gain of the inverter.

Figure 3(a) shows a schematic of our proposed self-bias inverter (SBI). The SBI consists of two inverters. The output voltage of the feedback inverter is connected to the body of

the main inverter. When V_{IN} is low, V_{OUT} and the output voltage of the feedback inverter become high and low, and $V_{TH,P}$ and $V_{TH,N}$ become low and high, respectively. Therefore, ΔV_{TH} is higher than 0 V ($\Delta V_{TH} > 0$). On the other hand, when V_{IN} is high, V_{OUT} and the output voltage of the feedback inverter become low and high, and $V_{TH,P}$ and $V_{TH,N}$ become high and low, respectively. Therefore, ΔV_{TH} is lower than 0 V ($\Delta V_{TH} < 0$). Thus, the VTC of our SBI comes close to two curves and the voltage gain is significantly improved, as shown in Fig. 3(b). The voltage gain of the SBI can be calculated as

$$|A_{INV}|_{MAX} = \left\{1 - \frac{1}{2}\frac{\partial(\Delta V_{TH})}{\partial V_{IN}}\right\}\left\{e^{\left(\frac{V_{DD}}{2V_T}\right)} - 1\right\}/\eta. \quad (2)$$

As shown in Eq. (2), the voltage gain is improved because $\partial(\Delta V_{TH})/\partial V_{IN} < 0$.

3. Experimental Results

We fabricated a proof-of-concept chip of our proposed ROSC (Prop.) using a 0.18-µm, 1-poly, and 6-metal CMOS technology. The conventional ROSC (Conv.) was also fabricated in the same chip. Figure 4 shows a micrograph of our chip. The Prop. and Conv. used 31 and 51 inverters, respectively, to obtain the same frequency. The areas of Prop. and Conv. were 0.015 and 0.0029 mm^2, respectively. In the measurement, we used source followers to sufficiently drive off-chip parasitics (bias current was set to 500 nA).

Figure 5 shows the measured waveforms of (a) Conv. and (b) Prop. at V_{DD} = 60 mV. The amplitudes of the proposed and conventional ROSCs were 52.0 and 41.9 mV, respectively. Higher amplitude was obtained by using our proposed SBI. Figure 6 shows the measured normalized amplitude as a function of V_{DD}. The proposed ROSC could oscillate at extremely low supply voltage of 42 mV, while the conventional one at 49 mV. Figure 7 shows the measured frequency and power consumption as a function of V_{DD}. Measured frequency and power consumption of our proposed ROSC were slightly slower and higher than those of the conventional one because the parasitics increased due to the additional circuits.

For comparison, Tab. I summarizes the performance of the proposed ROSC and others [1]-[3]. Our proposed ROSC achieved the lowest minimum supply voltage, 42 mV.

4. Conclusions

In this work, we propose an ROSC capable of operating at extremely low supply voltage. The proposed ROSC consists of gain-enhanced self-bias inverters. Measurements of a prototype chip demonstrated that the proposed ROSC can operate at extremely low voltage of 42 mV.

Acknowledgements

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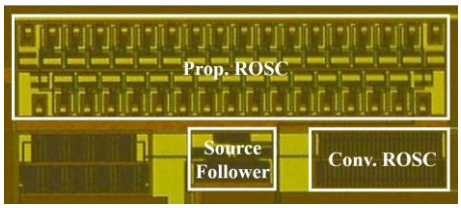
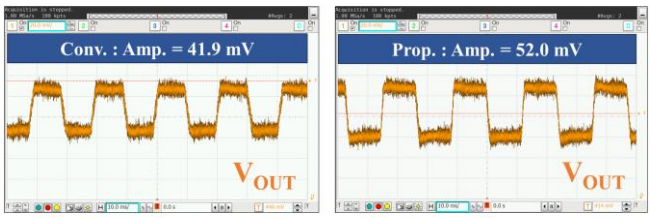


Fig. 4 Chip micrograph.



(a) (b)

Fig. 5 Measured waveforms of (a) Conv. and (b) Prop. at V_{DD} = 60mV.

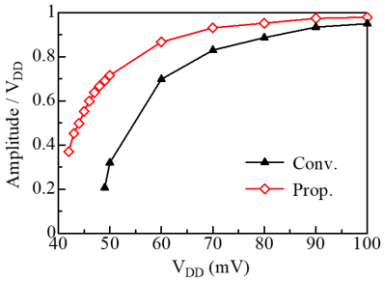
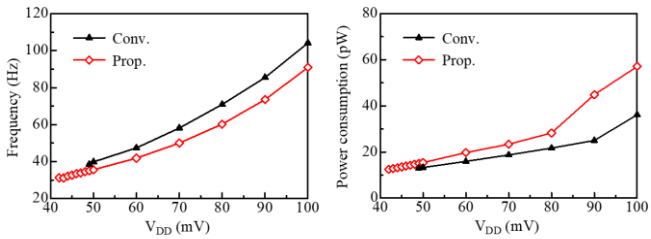


Fig. 6 Measured normalized amplitude of ROSCs as a function of V_{DD}.



(a) (b)

Fig. 7 Measured (a) frequency and (b) power consumption of the ROSCs as a function of V_{DD}.

Table I Performance comparison.

Ref.	Inverter type	Process	Min. V_{DD}
[1]	V_{TH}-tuned inverter	65 nm	82 mV
[2]	Selective schmitt-trigger inverter	0.13 µm	70 mV
[3]	Stacked inverter	0.18 µm	57 mV
This work	Self-bias inverter	0.18 µm	42 mV

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