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Packaging of SiC power device for miniaturization of power electronics system - fast switching operation and thermal management -

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Abstract

The packaging and fabricating technology of power module is important in miniaturization of power electronics system with utilizing fast switching and high current density capability of SiC power device. This paper develops power module substrate, which has low parasitic inductance in the wiring to mitigate over voltage stress on power device and to reduce EMI noise. Moreover, higher heat dissipation capability is achieved to deal with increasing exothermal density for power density growth of power module.

1. Introduction

The power electronics is expected as the measure for energy saving. The SiC unipolar power device is expected to have less conduction loss and faster switching operation than conventional Si bipolar power device [1]. The reduction of conduction loss attains high current density of power device and results in miniaturization of power module. The enhancement of switching speed actualizes high frequency switching operation and bring in downsizing of passive component to have same impedance and susceptance, respectively for inductor and capacitor. However, miniaturization of power module raises the thermal density. Then, it requires the improvement of heat dissipation capability of power module. The interaction of parasitic inductance in the wiring of power module and fast switching operation of power device induces surge voltage and EMI noise resulting from voltage and current oscillation [2]. Then, the reduction of parasitic inductance in power module is necessary for fast switching operation. This paper develops multilayer ceramic substrate of power module to realize low parasitic inductance and high thermal dissipation capability. The electrical performance of developed power module is experimentally evaluated with implementing SiC power device.

2. Developed power module substrate

Structure of power module substrate

Figure 1 shows the structure and circuit diagram of developed power module substrate. It has half bridge circuit configuration. Si_3N_4 is used as the base insulating ceramic material. The wiring layer consist of Cu, which is brazed with active metal on the ceramic substrate. The vacuum brazing enables void free adhesion. The developed multi-layer substrate is fabricated with bonding single layer substrates. The ceramic substrate buried large diameter via filled with Cu core, which conducts large current between surface and middle layer. Then, the middle Cu layer can be utilized as the current conduction path. The distance between surface and middle layer conductors is the thickness of ceramic substrate and constitutes small loop area for current path, when current is designed to reciprocate through surface and middle layer. Then, the parasitic inductance in the wiring of substrate results in small. The low parasitic inductance mitigates the occurrence of surge voltage and ringing oscillation of voltage and current accompanied by fast switching operation. The developed substrate has two ceramic layer, which has larger thermal resistance than Cu. The multi-stratification may deteriorate thermal performance.

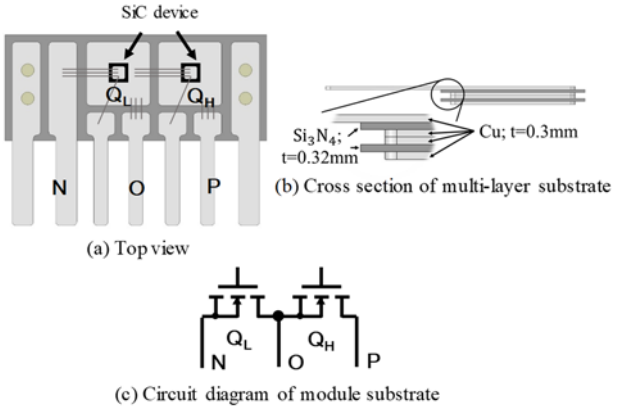
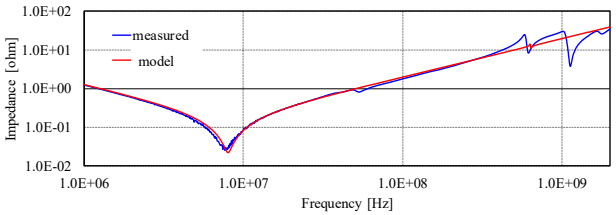
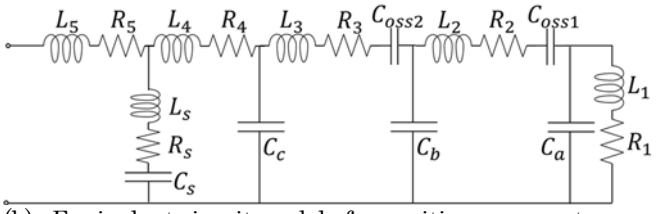


Fig. 1 Configuration of multilayer power module substrate.



(a) Frequency characteristics of impedance



(b) Equivalent circuit model of parasitic component

Fig. 2 Frequency characteristics of impedance for multilayer power module substrate.

Characterization of electrical performance

The frequency characteristics of impedance for the developed substrate is characterized and modeled as equivalent circuit. The lands on the substrate is directly wire bonded to exclude the characteristics of power device in the measurement. The equivalent circuit model is estimated from the topology of substrate as shown in Fig. 2(b). The parasitic inductances and capacitances are modeled with lumped element, which are identified to minimize mean square error in frequency characteristics of impedance. The modeled frequency characteristics of impedance is also shown in Fig. 2(a). The identified model well expresses the impedance up to 200MHz.

Characterization of thermal performance

This subsection characterizes transient thermal response of developed substrate as the thermal performance. The test is performed with the static test method, which is standardized as JEDEC JESD51 [3]. The transient thermal characterization of power module with SiC MOSFET has difficulty, due to dynamic gate threshold voltage shift [4]. Then, the test is performed with SiC SBD. The dynamic thermal model of the substrate is extracted from time response of junction temperature and expressed by structure function as shown by integral in Fig. 3.

The interface of die, die attach, Cu wiring, ceramic substrate, and heat sink give inflection in structure function, which is emphasized by differentiating obtained structure function. The results show that the thermal resistance of multilayer substrate is less than single layer substrate. The developed multilayer substrate has thick middle conductor layer, which stems from bonded single layer substrate structure. This thick middle conductor layer acts as the heat spreader and expands thermal conduction area. The increment of thermal resistance stemming from multiplication of ceramic substrate is overcame by the expanded thermal conduction area. The developed multilayer substrate reduces thermal resistance and improves thermal performance.

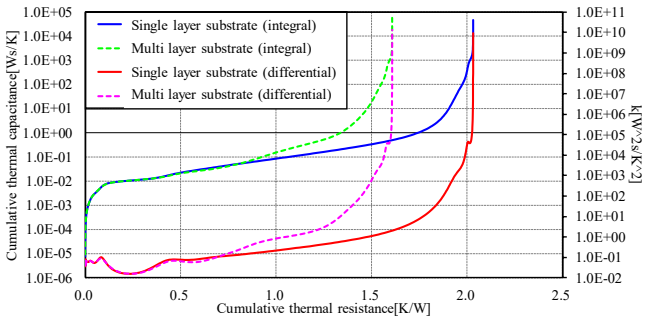
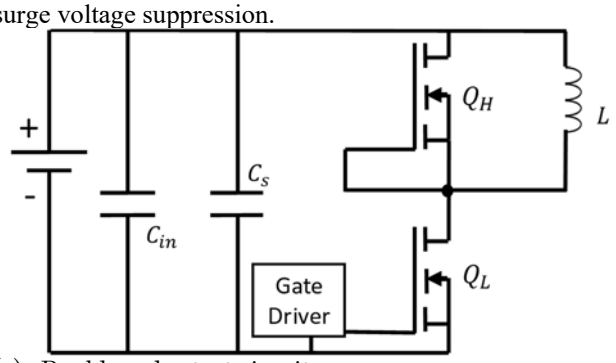


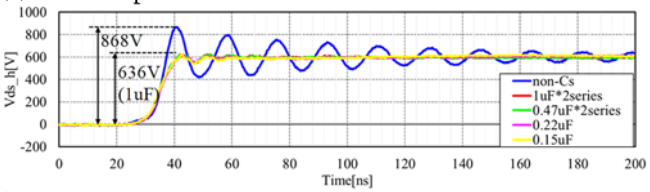
Fig. 3 Transient thermal characteristics of power module substrate.

3. Evaluation of module substrate in experimental circuit

The performance of developed SiC power module substrate is evaluated with the double pulse test circuit in Fig. 4(a), and the time response of voltage on SiC device in switching transient is assessed. The snubber capacitor built in the module substrate, and its capacitance is changed as a parameter. The experimental result is shown in Fig. 4(b). The parasitic inductance in the wiring between dc capacitor and half bridge is large. Then, large surge over voltage is observed, when snubber capacitor is not implemented. The built in snubber capacitor suppresses the surge voltage. The improvement of surge voltage suppression decreases for larger snubber capacitance. Then, snubber capacitance single digit larger than output capacitance Coss of MOSFET is sufficient for surge voltage suppression.



(a) Double pulse test circuit.



(b) Drain voltage response.

Fig. 4 Electrical transient response in switching operation.

3. Conclusions

This paper developed power module substrate to realize fast switching operation and high current density of SiC device. The multi-stratification of ceramic substrate shrinks the loop area of current conduction path and reduces its parasitic inductance in wiring. The heat dissipation capability of the module substrate is enhanced by the middle conductor layer. The built in snubber capacitor on the developed power module substrate effectively suppresses surge voltage accompanied by the fast switching operation, which is experimentally confirmed.

Acknowledgements

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