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Compact Modeling and Circuit Simulation for High-Power Devices

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Abstract

Circuit simulation involving high-power devices require compact models that consider physical phenomena occurring when device structures and materials to sustain the internal high electric field are employed. This paper presents the features of extending a Si-based high-voltage model to consider the resistance effects due to varying structures and material properties. Comparisons with 2D device simulation and measurement are used to validate the developed model for SiC. Circuit simulation and prediction of circuit efficiency degradation due to device aging are presented, where measurements are typically not available.

1. Introduction

Semiconductor device performance has progressed toward high current density, high electric field and faster switching speed for high power applications. To realize such performance, devices have undergone changes in device structures, shown in Fig. 1, and/or materials to sustain the high electric field in the channel. Such advances enabled achievement of high blocking voltage as summarized in Table I. Understanding new occurring physical phenomena [1] along with these advances become a requirement for device and circuit engineers. For this purpose, accurate physics-based compact modeling is necessary. While extension of the high-voltage HiSIM_HV offers a straightforward solution, specific features of high-power device structures and materials need to be fulfilled:

i. *Modeling of internal resistance effect.* Trench-type and super-junction structures modulate the resistance in the *n*-layer that determine the high-voltage characteristics.
ii. *Different material properties* as shown in Table II. SiC, on the otherhand, is well-known to have a much higher density of states compared with Si [2]. Additional task is:
iii. *Influence of SiC/SiO_2 interface traps.* The high magnitude ($\sim 10^{12}$cm^{-2}eV^{-1}) of integrated defect density D_{it} degrades the electrical characteristics and leads to device aging.

Our aim is to develop high-power device models by preserving the surface-potential approach of HiSIM_HV and extending the modeling of the resistance part to fulfill the requirements listed above.

2. Compact Modeling of High Power Devices

i. *Modeling of internal resistance effect.* HiSIM_HV solves the Poisson equation self-consistently to describe the device current and capacitance characteristics. The resistance effects (denoted by the red box in Fig. 1) and its modulation that sustains the high electric field inside the device is modeled consistently inside HiSIM_HV formulation. The potential distribution along the channel with the important nodes to be solved are shown in Fig. 2 [3].

ii. *Different material properties.* Fig. 3 shows the effect of changing the material properties and impurity concentration of a HV model from Si to SiC. To validate the applicability of the model, the electrical characteristics of a commercially available SiC MOSFET with V_{dd}=500V is shown in Fig. 4. Reproduction is achieved. For the mobility, universal mobility that is observed in Si-based device is not strictly followed. The effect of high density of trap states is phenomenologically modeled by the strength of the phonon scattering [4].

iii. *Influence of SiC/SiO_2 interface traps.* 4H-SiC/SiO_2 interface defect density is characterized by distinct deep and shallow traps. Although processes have eliminated the deep trap states, the shallow trap states are still dominating as shown by recent measurements [5]. To model the effects of the trap density N_{trap}, the Poisson equation solved in the model is modified to include N_{trap}. The trap/detrap of carriers is also modeled as in [6]. Fig. 5 shows the schematic of modeling the trap density increase.

3. Simulation Example of Power Loss with SiC model

A switching circuit with high voltage MOSFET and a free-wheeling diode in Fig. 6(a) is simulated. Results for gate switch-on and switch-off are shown in Fig. 6(b) and 6(c), respectively. At switch-on, the carrier trap density builds up which results to delay in I_{ds} increase and a delay in the V_{ds} reduction. At switch-off, the effect of trap is to decrease the delay. The remaining trap density increases the threshold voltage which reduces the effective gate voltage. The simulated power loss predicts the measurement as in Fig. 7. The broadened switching power loss suggests enhanced effect of traps and relates to long-term reliability problems.

4. Simulation Example of Aging with SiC model

To demonstrate the capability of predicting degradation due to interface traps, the I_{ds}-V_{gs} stress measurements [7] in Fig. 8 are used. During DC Fowler-Nordheim (FN) stress, carriers are injected into the gate for different stress durations of 30s, 90s and 360s. Current degradation, characterized by higher gate voltage and smaller magnitude, becomes more evident as stress is prolonged. The efficiency of a DC-AC converter circuit in Fig. 9 is calculated for different stress times. A substantial reduction of 10% occurs after a stress time of 360s in Fig. 10. Such model capability of predicting degradation is necessary where measurements are usually not available [8].

5. Summary

The requirements of extending existing compact models to high-power structures and different materials are presented. Developed model for SiC-based material is verified to reproduce DC and AC measurement results. Stable transient simulation is presented with capabilities of predicting circuit efficiency degradation due to aging by carrier traps.

References

[1] W. J. Choyke, et al., Springer, 2004. [2] D. Navarro, et al., JJAP 56, 2017.
[3] https://www.hisim.hiroshima-u.ac.jp/ [4] A. Saito, et al. IEICE Vol. E99-C, 2016.
[5] H. Shiomi, et al, JJAP 55, 2016. [6] Y. Tanimoto, et al, IEEE Pow. Elec. 31, 2016.
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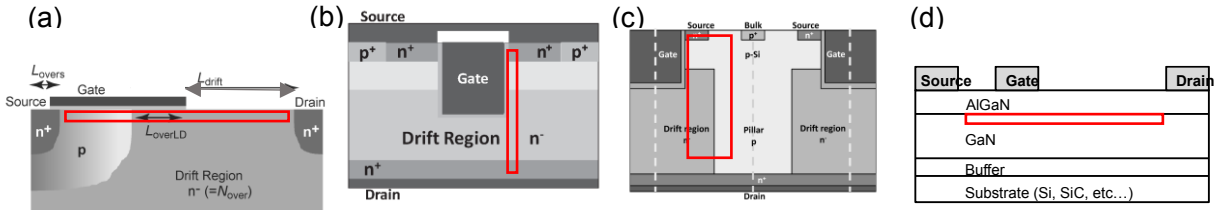

Fig. 1. (a) LDMOS (b) Trench structure (c) SJMOS structure (d) GaN-HEMT.

Table I. High-Power Device Structures

Material	Device Structure	Designed Blocking Voltage
Si	LDMOS	50V (NXP)
	Trench-gate	500V (General Electric)
	Super Junction	600V (Fuji Electric)
	IGBT	1000V
SiC	Trench-gate	1200V (Infineon)
GaN	HEMT	600V (Toshiba)

Table II. Material Properties

	Si	4H-SiC	GaN
Bandgap energy (eV)	1.1	3.26	3.4
Intrinsic Carrier Density (cm^{-3})	1.45×10^{10}	9.7×10^{-9}	1.9×10^{-10}
Dielectric constant	11.9	10.1	9

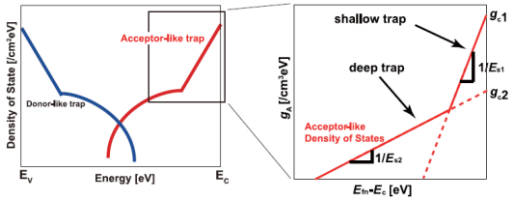

Fig 5. Schematic representation of modeling the interface traps.

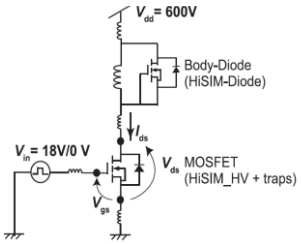

Fig. 6(a). Switching circuit with high-voltage MOS.

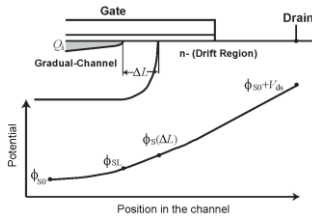

Fig. 2. Potential distribution along the channel.

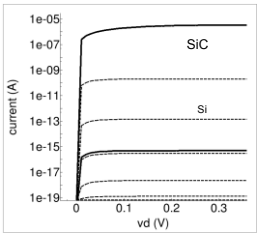

Fig. 3. Effect of changing material property and impurity concentration.

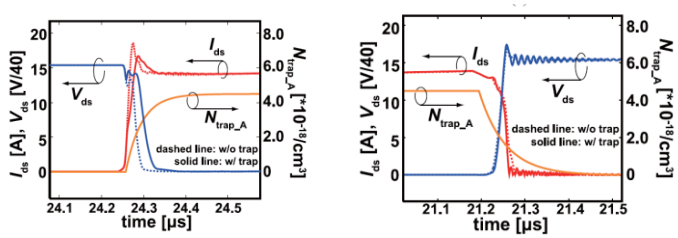

Fig. 6(b) and (c). Switch-on and switch-off characteristics with and without traps.

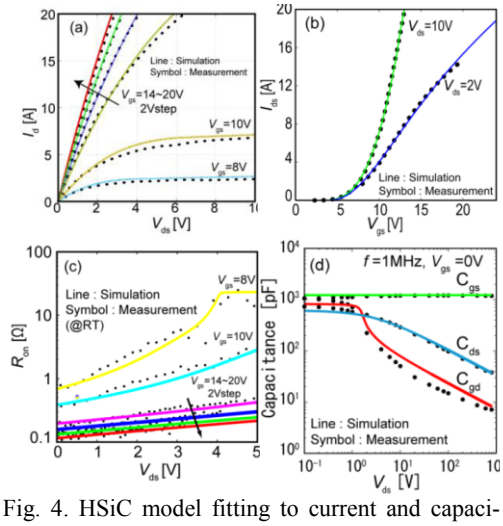

Fig. 4. HSiC model fitting to current and capacitance measurement data.

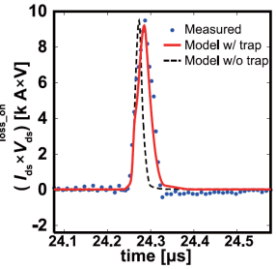

Fig. 7. Power loss calculation with and without trap.

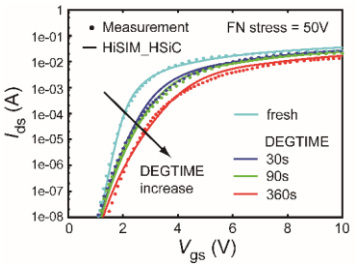

Fig. 8. Measured I_{ds} characteristics with stress applied for different times.

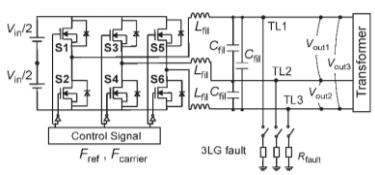

Fig. 9. DC-AC Converter circuit.

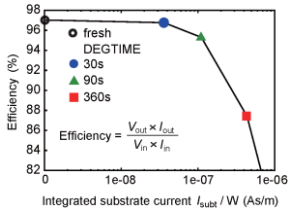

Fig. 10. HSiC-calculated converter circuit efficiency.