Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp545-546

Nano-Watt Voltage References with Sub-10 ppm/°C Temperature Coefficients

Chun-Shiang Dai and Hongchin Lin

Dept. of Electrical Engineering, National Chung Hsing University, Taichung, Taiwan
Phone: +886-4-2284-0688 ext. 808 E-mail: hclin@nchu.edu.tw

Abstract

A voltage reference circuit with all transistors biased in subthreshold generating a reference voltage of 240.4 mV with power consumption of 1.14 nW at the supply voltage of 0.65 V is proposed. The temperature coefficients (TC) of the circuits without and with trimming are 4.2 and 8.56 ppm/ºC, respectively, for temperatures from -20 to 120 ºC. The line sensitivity (LS) is 0.162%/V for the supply voltages from 0.65 to 2 V. It was implemented using the 0.18 μm CMOS technology.

1. Introduction

Voltage references are widely used in integrated circuits to generate a DC voltage independent of process, supply voltage and temperature (PVT) variations. The conventional solution is the BJT-based bandgap voltage reference (BGR). The bandgap of around 1.2 V in silicon limits low voltage and ultra-low power operation [1]. Thus, employing subthreshold of MOSFETs to produce reference voltages is getting popular in recent years. The MOS-only voltage reference in [2] only utilizes normal-voltage (NV) MOSFETs to achieve high-slope proportional-to-absolute temperature (PTAT) generators to reduce the number of stages compared to [1]. However, stacking several MOS transistors results in higher supply voltages, power consumption and area.

The other type of subthreshold operation employing NV and high-voltage (HV) MOSFETs to generate the reference voltage (V_{REF}) using the difference of threshold voltages (V_t) of HV and NV MOSFETs to reduce both the power consumption and the supply voltage [3] but the performance of TC and LS is degraded owing to V_{REF} obtained by one diode-connected NV MOSFET. The V_{REF} using only one NV plus one native transistor can achieve ultra-low power of only tens pico-watt [4]. However, to cope with process variation, it utilized the one-time-programmable (OTP) trimming technique to avoid the influence of leakage with extra cost.

2. Proposed Voltage Reference

The proposed voltage reference comprises a start-up, a current generator and an active load. The start-up circuit and current generator with the aspect ratios are given in Fig. 1. The active loads with and without trimming generating the reference voltages V_{ref1} and V_{ref2} are shown in Figs. 2(a) and 2(b), respectively. The current generator [3] is composed of one HV MOSFET with the symbol having a bold line at the gate and four NV MOSFETs. I_{M4} is copied to I_{M6}, which is

$$I_{M6} = r_{64} Q^{1/\Sigma} \mu V_T^2 \exp\left(-\Delta V_t / V_T \Sigma\right)$$

where $r_{64} = I_{M6}/I_{M4}$, $Q = r_{54}^{m_H - m_N}\left(S_{M3}^{m_N} S_{M1}^{m_N} / S_{M2}^{m_H}\right)$, $\Sigma = 2m_N - m_H$, and $\Delta V_t = V_{t1} + V_{t3} - V_{t2}$. Besides, m_N and m_H are the subthreshold slope parameters of NV and HV MOSFETs; S_{M1} to S_{M3} are the aspect ratios of M1 to M3; μ is the mobility for all n-MOS transistors, $V_T = k_B T/q$ and $r_{54} = I_{M5}/I_{M4}$.

Unlike the active load in [3] using an n-MOSFET, a NV and a HV transistor to generate V_{REF} as shown in Fig. 2(a), which features the similar biases at the drains of M3 and M7 to improve the TC and LS. The resulting $V_{REF} = V_{GS8} - V_{GS7}$ is

$$V_{REF} = V_{t8} + m_H V_T \ln\left(I_{M6}/\mu_H C_{oxH} S_{M8} V_T^2\right) - \left[V_{t7} + m_N V_T \ln\left(I_{M6}/\mu_N C_{oxN} S_{M7} V_T^2\right)\right]$$

By setting $\partial V_{REF}/\partial T = 0$, it can be found if the size ratio $S_{M8}^{m_H}/S_{M7}^{m_N}$ satisfies some relationship and the size selection is flexible for trimming, the ideal V_{REF} can be expressed as

$$V_{REF} = \frac{m_N}{2m_N - m_H}\left(V_{tH}(T_0) - k_H\right) - \frac{m_H}{2m_N - m_H}\left(V_{tN}(T_0) - k_N\right) + k_N'\left(V_{BS7} + \frac{m_H - m_N}{2m_N - m_H} V_{BS3}\right),$$ where k_N and k_H are the TC of V_t.

The process variation influences the value of V_{REF}, the conventional on/off current paths may degrade the TC and LS owing to leakage current of subthreshold. Here, we propose the digital trimming technique without turning off the active loads using combination of NMOS switches (d1 ~ d3) as shown in Fig. 2(b) to tune V_{REF} from 232 to 248 mV.

3. Simulation and Implementation Results

The proposed nano-watt V_{REF} circuits with (V_{ref2}) and without (V_{ref1}) digital trimming were fabricated using the TSMC 0.18 μm CMOS technology. The die microphotograph is shown in Fig. 3. The TCs of V_{ref1} at various V_{dd}'s could be as low as 4.2 ppm/ºC as shown in Fig. 4. The power dissipation is as low as 1.14 nW at V_{dd} = 0.65 V. Figure 5 demonstrates slight variation of V_{REF} when V_{dd} varying from 0.65 to 2 V. The LS of V_{ref1} is 0.162%/V at room temperature. The V_{REF}'s with trimming (V_{ref2}) keep the ultra-low TCs for various trimming conditions as shown in Fig. 6. Likewise, the various V_{ref2} curves of different trimming conditions keep the low LS for V_{dd} from 0.65 to 2 V at room temperature. Table I summarizes the performance of V_{ref1} and V_{ref2}.

4. Conclusions

Table II compares performance of some tens-nW or lower voltage references. The proposed configuration featuring simple trimming capability achieves the lowest TC also has good LS owing to identical topologies of the current generator and the active load. Moreover, the proposed circuits preserve nano-watt power dissipation and tiny die area.

References

[1] Y. Osaki *et al.*, IEEE J. Solid-State Circuits **48** (2013) 1530.
[2] H. Zhang *et al.*, IEEE Trans. CAS II **65** (2018) 1.
[3] L. Magnelli *et al.*, IEEE J. Solid-State Circuits **46** (2011) 465.
[4] M. Seok *et al.*, IEEE J. Solid-State Circuits **47** (2012) 253.

Acknowledgements

The authors would like to acknowledge the Taiwan Semiconductor Research Institute (TSRI) of the National Applied Research Laboratories (NARL) of Taiwan for the support in chip fabrication. This work was supported by Ministry of Science and Technology of Taiwan (MOST 106-2221-E-005-084).

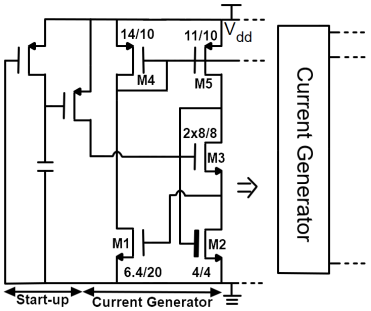


Fig. 1 The current generator for the active load to produce V_{REF}

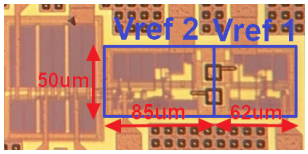


Fig. 3 The die microphotograph

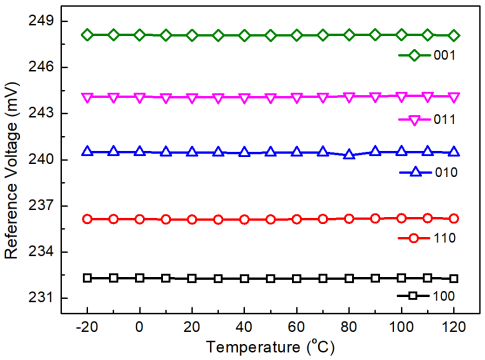
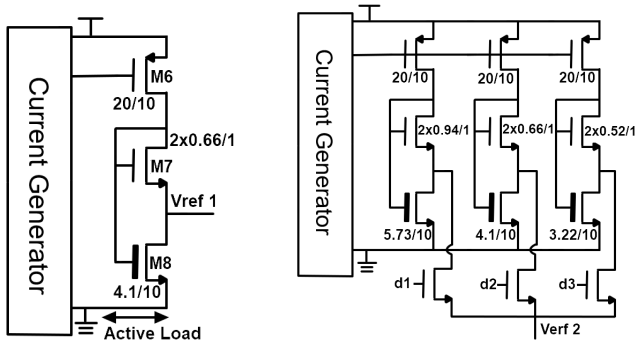


Fig. 6 V_{ref2} with trimming vs. temperature at V_{dd} = 0.65 V



(a) no trimming (V_{ref1}) (b) with trimming (V_{ref2})

Fig. 2 The proposed CMOS voltage references (a) V_{ref1} and (b) V_{ref2}

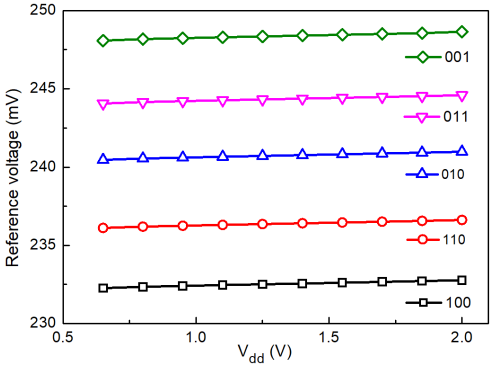


Fig. 7 V_{ref2} with trimming vs. V_{dd} at room temperature

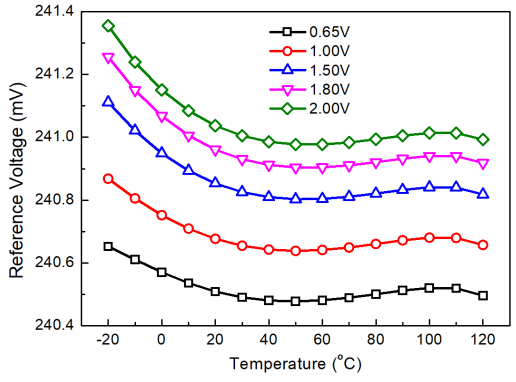


Fig. 4 V_{ref1} slightly dependent on temperature

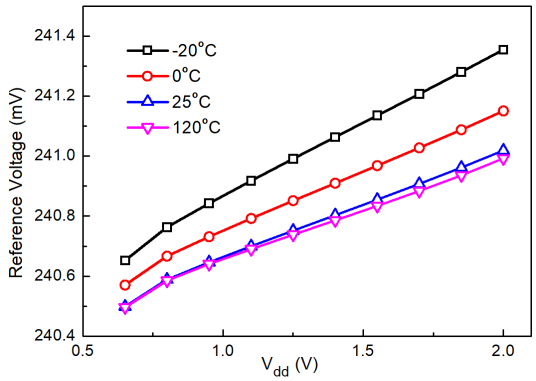


Fig. 5 V_{ref1} slightly dependent on supply voltages (V_{dd})

Table I Performance of V_{ref1} and V_{ref2} after trimming

Supply voltages (V)	0.65 to 2					
Power (nW)	1.14	2.14				
d1 d2 d3	NA	100	110	010	011	001
V_{REF} (mV)	240.4	232.2	236	240.4	244	248
TC (ppm/°C)	4.2	8.13	5.92	8.56	5.42	8.59
Temperatures (°C)	-20 to 120					
LS (%/V)	0.1618	0.1618	0.1613	0.1625	0.1618	0.1629
PSRR (dB) 100Hz	-58.72	-58.97	-58.42	-57.78	-57.29	-56.64
10MHz	-56.56	-57.19	-51.92	-58.33	-52.92	-59.26
Area (mm^2)	0.0031	0.00425				

Table II Comparison with the low-power CMOS voltage references

	[1]	[2]	[3]	[4]	V_{ref1}	V_{ref2}
Technology (μm)	0.18	0.18	0.18	0.13	0.18	
Supply voltages (V)	0.7-1.8	1-1.8	0.45-2	0.5-3	0.65-2	
Power (nW)	52.5	23	2.6	0.0055	1.14	2.14
V_{ref} (mV)	548	756	263.5	174.9	240.4	240.4
TC (ppm/°C)	114	49.6	142	16.9	**4.2**	**8.56**
Temperatures (°C)	-40-120	-40-125	0-125	-20-80	-20-120	
LS (%/V)		0.524	0.44	0.033	0.162	0.162
PSRR(dB) 100Hz	-56	-52	-45	-53	-58.72	-57.78
10MHz			-12.2	-62	-58.56	-58.33
Die area (mm^2)	0.0294	0.0162	0.043	0.00135	0.0031	0.00425