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Enabling Ultra Low-Vmin and Low-Leakage Operation in FDSOI High-density SRAMs

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Abstract

An extensive study of key parameters impacting SRAM Vmin is described in this paper, showing the benefit of using FDSOI technology with optimized SRAM architecture and bitcell centering. The path allowing sub-0.6V Vmin for 28nm FDSOI technology with Single-Port High-Density (SPHD) bitcells is presented. Finally, different ways to obtain leakage below 1pA are showed, thus enabling very low power consumption in Stand-By mode and reinforcing the high potential of FDSOI technology to hit ultra low voltage markets.

1. Introduction

Embedded memories play a key role to enable applications for Mobile, Internet of Things and System-on-Chip (SoC). Conventional 6T-SRAM are the most common type of storage memories: they take up to 20-30% area of SoC and consume 40-50% of total chip power. Concerning area, SRAM 6T bitcells have been scaled by nearly 2 orders of magnitude from 0.13µm to 7nm technologies [1], thanks to continuous innovations in process technology and design solutions. Reducing SRAM power dissipation is critical to improve the total SoC power consumption. Lowering memory supply voltage during active operation is the most efficient knob to reduce dynamic power. As SRAM minimum supply voltage does not scale as much as logic [2], SRAM Vmin is becoming a system bottleneck.

2. SRAM Vmin definition and challenges

SRAM Vmin is defined as the minimum supply voltage for which the memory cut remains functional. With cell size scaling, increased variability appears at Low-Vdd and Yield drop is observed with Vdd reduction due to a Read or Write operation failure [Fig.1]. Failure sensitivity is emphasized by global and local fluctuations (device variability & mismatch).

The fundamental limitations faced by SRAM Vdd scaling are due to conflicting requirements for Read and Write operations. Indeed, as Static Noise Margin (SNM) and Write Margin (WM) optimization takes opposite directions [Fig.2], a very tiny operating window is obtained at low-Vdd, as reported in [3-6]. Finally, during stress applied to products, Vth of SRAM Pmos increases with time due to NBTI degradation. As SNM degradation is a consequence of NBTI drift, only Read limited bits drift during stress [7], thus showing the key role played by initial bitcell centering in ageing behavior, as shown in Fig3.

3. Vmin optimization in FDSOI High-Density bitcells

FDSOI offers a very competitive technology for Low Voltage SRAM applications due to improved electrostatic control [8] and low local mismatch variability due to undoped channel [9]. Thanks to specific bitcell biasing enabled by FDSOI & single p-well benefits [10], the single p-well SRAM architecture is selected in 28nm FDSOI technology as the best solution for Vmin lowering (Fig.4).

SRAM Vmin is a function of large amount of parameters, which are reported in Table I. A typical Vmin curve on SPHD vs temperature is showed in Fig.5. Minimum voltage supply is limited by WM at low temperature and by SNM at high temperature, with an increase up to 100mV with respect to Vmin measured at room temperature. The impact of Nmos/Pmos process centering is showed in Fig. 6-7. SNM is efficiently modulated thanks to Vth NP tuning, thus showing clear shape change in Vmin curve for Write limited bitcells [11]. Additionally, Vmin increases with memory cut size, and the amount of shift still depends on bitcell centering, as show in Fig.8.

The percentile used to assess the minimum supply voltage plays also a key role, as low ppm requirements are very critical to be proven on silicon, especially at early technology development stage. Finally, Vmin drift during operating stress, defined by mission profile, has to be taken into account for final product functionality. As shown in Table II, there is a quite significant gap between product requirements and what can be easily measured on silicon [11]. For this reason, the accurate Vmin simulation approach described in [12] help to provide guidelines to guarantee End-Of-Life SRAM Vmin for products considering its usage conditions and memory capacity.

Other constraints such as speed or low leakage requirements can guide the bitcell centering (cf. N-fast for speed, N-slow for low leakage), but still low voltage functionality is required. In this case, design assist techniques such as Read or Write assist can be used, depending on product usage [13]. Thanks to appropriate bitcell centering and the usage of Write Assist, Vmin of 0.6V and 0.5V is showed for 0.120µm² and 0152µm² bitcells respectively (Fig.9).

Finally, a unique opportunity offered by FDSOI is the possibility to modulate dynamically bitcell centering, together with SNM and WM, w/o design assist, by simply using body biasing [14-15]. With BB, bitcell centering can be efficiently tuned from SF (in RBB mode) towards FS (in FBB mode), thus enabling the achievement of lower Vmin in worst case temperature. As shown in Fig.10, FBB is used to recover Vmin for a Write limited bitcell at -40°C.

4. Ultra Low Leakage SRAM guidelines

Inside SoC, retention areas must be optimized for the lowest power consumption in Stand-By mode. Thanks to very low Vmin retention demonstrated in [12], stand-by leakage is significantly reduced (Isb x0.7) at 0.4V compared to standard values of 0.6V. Further leakage lowering can be obtained with larger Lgate on SRAM and source biasing [16], as shown in Fig.11. The high interest of FDSOI for ultra low leakage applications is finally put into evidence by benchmark with 28nm node bitcells in Fig.12.

5. Conclusions

Guidelines to reduce SRAM operating voltage and leakage are extensively described in this paper. Silicon results on extended operating range (temperature, cut size, bitcell centering) are showed and simulations are used to predict product End-Of-Life Vmin. Different paths to reduce Stand-By leakage are explained, thus providing very competitive memories for ultra low power applications.

References [1] J. Chang et al, VLSI 2017 [2] T. Song et al, ISSCC 2014 [3] N. Planes et al, SSDM 2008 [4] K. Zhang et al, VLSI 2012 [5] Y. Yamamoto et al, VLSI 2013 [6] M. Yamaoka et al, ISSCC 2005 [7] J.C. Lin et al, IEDM 2006 [8] F.Arnaud et al, IEDM 2012 [9] N.Planes et al, VLSI 2012 [10] R. Ranica et al, VLSI 2013 [11] R.Ranica et al, S3S Shortcourse 2018 [12] R. Ranica et al, VLSI 2016 [13] M. Yabuuchi et al, ISSCC 2014 [14] P. Flatresse et al, ISSCC 2013 [15] F.Arnaud et al, S3S Conf. 2017 [16] T.Fukuda et al., ISSCC 2014

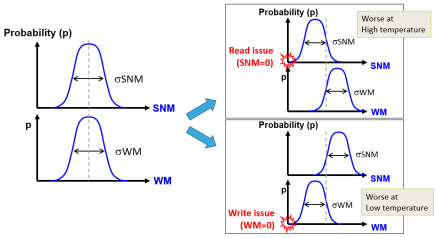

Fig.1: A bit fails at low voltage because of a Read or Write operation issue.

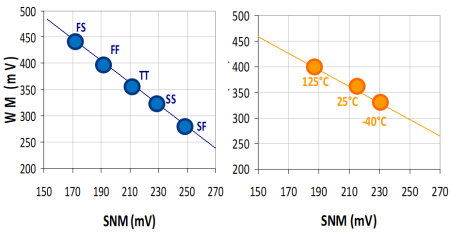

Fig 2: SNM and WM compromise vs NP centering and temperature.

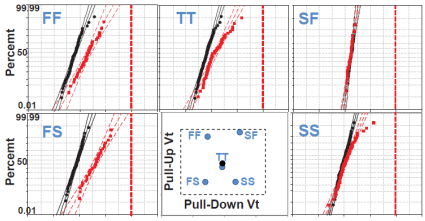

Fig 3: Impact of bitcell centering on Vmin drift: N-fast parts (FS and FF) are the most sensitive to ageing due to Read limitation.

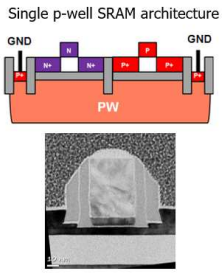

Fig 4: FDSOI SRAM architecture and SPHD 0.120µm² Nmos TEM.

Parameters impacting Vmin
Temperature range
Silicon centering
Memory capacity
Vmin percentile
Ageing

Table I: Key parameters impacting SRAM Vmin.

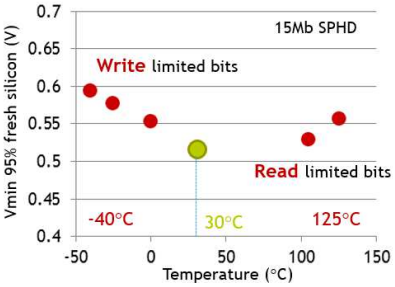

Fig 5: 15Mb SPHD Vmin measured on -40/125°C temperature range, showing Read-Write limitations.

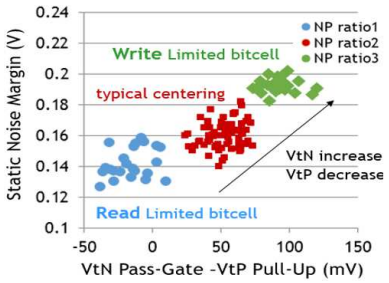

Fig 6: Vth Nmos (Pass-Gate) and Vth Pmos (Pull-Up) ratio is used to tune SNM from Read limited to Write limited bitcell.

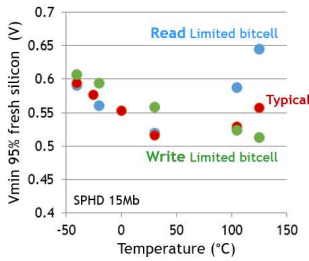

Fig 7: Vmin shape change on Write limited bitcells.

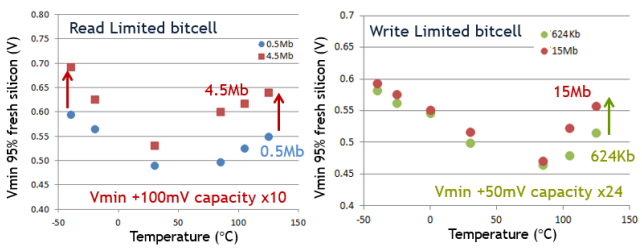

Fig 8: Vmin increases with memory capacity, depending on bitcell centering (Read-Write limited).

Parameters Impacting Vmin	Specifications	Silicon
Temperature range	0°C / 85°C consumer -20°C / 105°C networking -40°C / 125°C industrial -40°C / 165°C automotive	-40°C / 125°C most common range
Silicon centering	TT/FS/SF worst case	Read/Write limited
Memory capacity	Product size	Up to 128Mb in 28nm FDSOI
Vmin percentile	100ppm → 99.99% 1 ppm → 99.9999%	90-95% during Yield ramp-up
Ageing	Product Mission Profile	Fresh & aged

Table II: Product specifications and silicon status for Vmin evaluation.

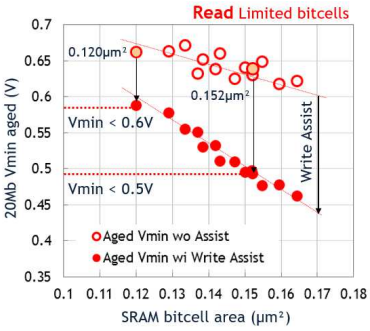

Fig 9: Vmin simulations with and w/o Write Assist vs bitcell area.

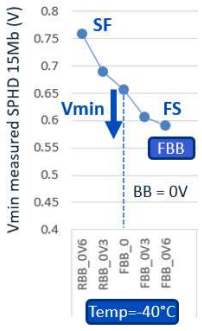

Fig 10:Vmin behavior vs BB at -40°C on a Write limited bitcell.

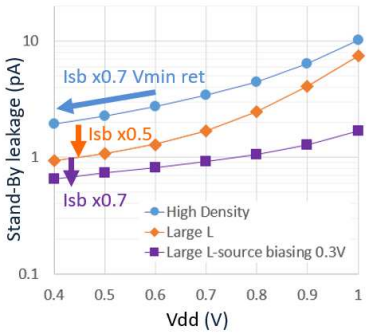

Fig 11: Stand-By leakage vs Vdd on SPHD & Large-L (+5% area) bitcell, combined with source biasing.

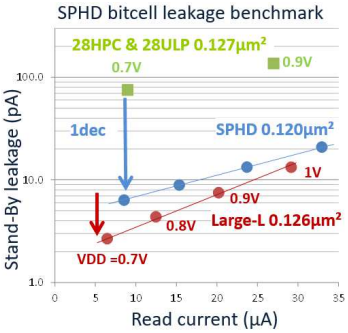

Fig 12: SRAM leakage benchmark at 28nm node showing high potentiality of FDSOI technology