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Self-Heating-Aware Cell Design for Multi-Stacked Circuits with p/n-Vertically-Integrated Nanowires on FinFET

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Abstract

Self-heating-aware design for multi-stacked circuits with p/n-vertically-integrated nanowire (NW) on FinFET is investigated for beyond 3-nm technology node. Based on the assumptions of process flow, area reductions are remarkably achieved for inverter, transmission gate, NAND, NOR and 6T-SRAM cells suppressing the self-heating effect (SHE) simultaneously.

I. Introduction

Single-nm-level CMOS devices as a key component of SoC are still being scaled along the technology roadmap for the IoT/AI society [1–5]. Fig. 1 shows a 6T-SRAM cell size on published year, which clearly shows that recent progress is being slower paces at 0.8^2-times per two years. As one of strong candidates, stacked NW [6–13] on FinFET has been proposed to suppress the self-heating effect [14] by recessed contact, as shown in Figs. 2 and 3 [15].

In this paper, multi-stacked circuits using p/n-vertically-integrated NWs on FinFET are investigated for cell area reduction and self-heating effect immunity.

II. Process assumptions

P/n-vertically-integrated NWs on FinFET has been assumed to be constructed as following process steps, starting with Si/SiO_2-laminated wafer, as shown in Fig. 4. Fin structure is formed by a shallow trench isolation (STI) process with a SiN liner underneath an SiO_2 film. As a self-aligned S/D formation, a fork contact hole is firstly formed [16]. After the etch-back and epi process for the bottom FET, a contact metal is formed by deposition and etch-back [17]. In contrast in epi process for top pFET, SiGe are performed for compressive stress. After dummy poly-Si removal, high-k and gate metal are formed for bottom- and top-layer of FETs, consequently. Finally, a diffusion break is yielded to cut unnecessary NWs.

III. Self-heating effect (SHE) reduction

To estimate electrical characteristics with the self-heating effect, saturation characteristics of p- and n-NW FETs are simulated using the ATLAS tool with thermal models. Fig. 5 shows the comparison between NW on FinFETs without and with recessed contact, in which the current degradation caused by the self-heating effect for both n and pFETs has been clearly suppressed by recessed contact.

IV. SHE-aware cell design

In term of the length from heat sink, multi-stacked pFETs are concerned. As stacked circuits, 2-input NAND with p/n-vertically-integrated NW/FinFETs is shown in Fig. 6. A thermal path from pFETs having an input of V_B are preserved through the electrode of V_{out} to silicon substrate. And also, this layout of 2-input NAND successfully results in an area size of $48F^2$, as compared to $80F^2$ of planar one.

2-input NOR cell is also investigated as shown in Fig. 7. A thermal path from pFETs having inputs of V_A and V_B is preserved through an electrode of V_{out} to silicon substrate. And also, this layout has an area size of only $56F^2$, as compared to $80F^2$ for planar one. Fig. 8 summarizes the cell area reduction depending on number of transistors including inverter, transmission gate and 6T-SRAM. The area-sizes of 3D layout are remarkably smaller than those of planar ones, especially when it consists of six or below.

However, the length from heat sink to pFETs is enlarged by the number of inputs especially in multi-stacked NOR cell. Fig. 9 shows drain conductance dependence on the number of stacked pFETs at V_{gs} of 1.0 V. The g_{ds} with 5 inputs in this proposed circuit is much higher than that with one input in thermally floated circuit. It is found that proposed technology enables area reduction in variety of cells even including multi-stacked circuits preserving the thermal flow path to suppress the self-heating effect.

V. Conclusions

SHE-aware cell configurations using p/n-vertically- integrated NW/FinFETs were proposed also for multi-input circuits. Based on the assumptions of process flow, a reasonable area reduction has been also designed for inverter, 6T-SRAM, transmission gate, NAND and NOR cells. The proposed p/n-vertically-integrated NW/FinFETs are considered to be strong candidates for beyond 3-nm node.

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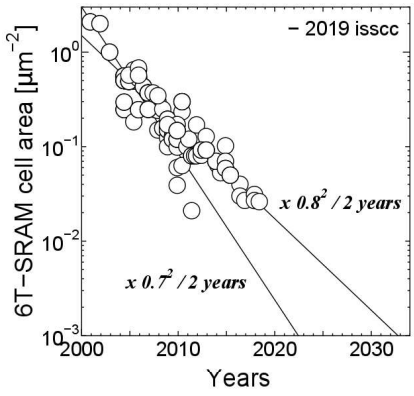

Figure 1: 6T-SRAM cell size dependence on year along x 0.7^2 and 0.8^2 per 2 years. Recent progress is being along with slower pacing.

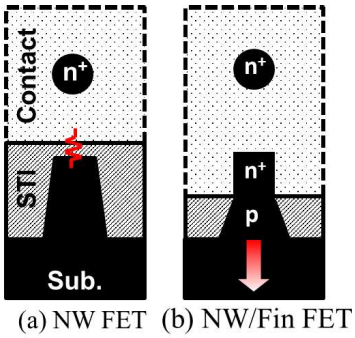

Figure 2: Schematic images on thermal current from nanowire (a) without and (b) with recessed contacts, which enables us thermal flow from nanowire to bulk silicon directly.

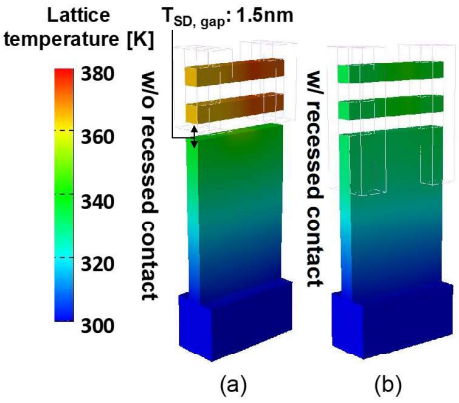

Figure 3: Lattice temperature images (a) without and (b) with recessed contacts, which enables us cooling of nanowire.

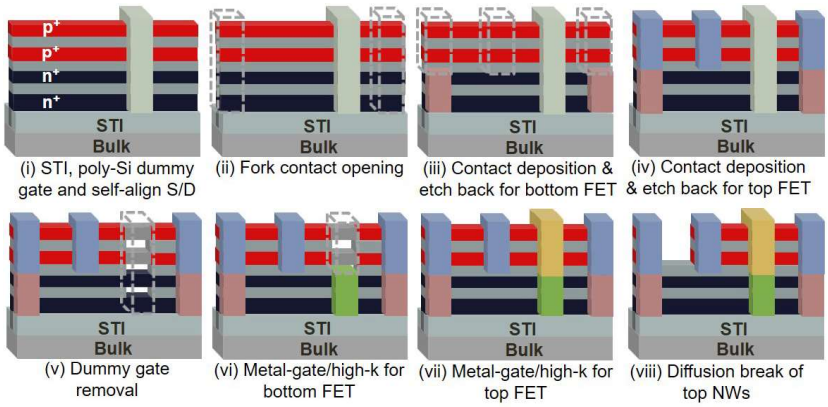

Figure 4: Assumption of process sequence for p/n-vertically-integrated nanowire on FinFETs.

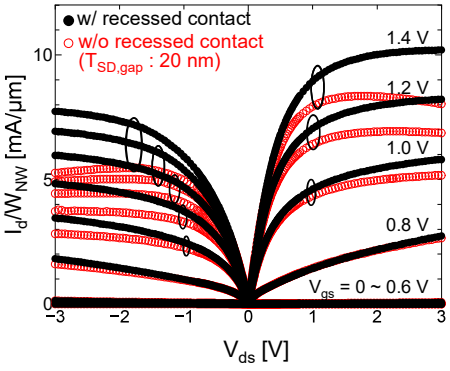

Figure 5: Simulated I_d-V_{ds} characteristics for single-NW on FinFET with and without recessed contact.

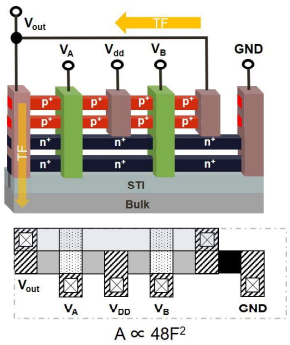

Figure 6: 3D configuration and 2D layout for 2-input NAND with p/n-vertically-integrated NW/FinFETs.

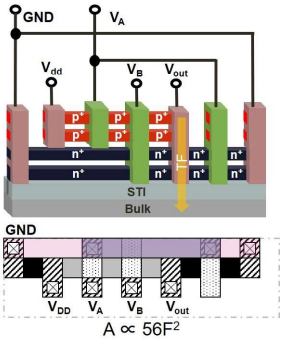

Figure 7: 3D configuration and 2D layout for 2-input NOR with p/n-vertically-integrated NW/FinFETs.

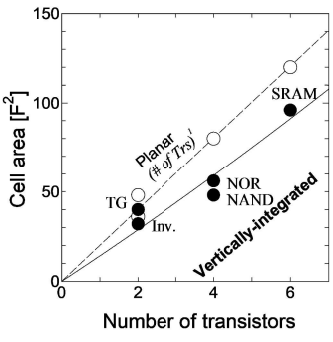

Figure 8: Cell area dependence on number of transistors for some of cell configurations. TG: Transfer gate, Inv.: Inverter.

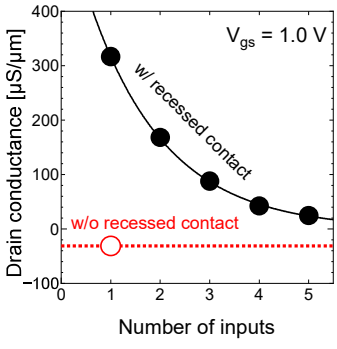

Figure 9: Simulated drain conductance dependence on number of inputs considering self-heating effects for multi-input NOR in Fig. 7.