Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp559-560

Scaled, Novel Effective Workfunction Metal Gate Stacks for Advanced Low-V_T, Gate-All-Around Vertically Stacked Nanosheet FETs with Reduced Vertical Distance between Sheets

A. Veloso[1], E. Simoen[1], A. Oliveira[2], A. Chasin[1], S.-C. Chen[3], Y. Lin[3], T. Miyashita[3], M. Kim[3], D. Jang[1], R. Ritzenthaler[1], X. Zhou[1], H. Mertens[1], V. Pena[4], G. Santoro[4], K. Kenis[1], F. Sebaai[1], G. Mannaert[1], K. Devriendt[1], T. Hopf[1], J. J. Versluijs[1], O. Richard[1], J. Machillot[4], N. Yoshida[3], and N. Horiguchi[1]

[1]Imec, Kapeldreef 75, 3001 Leuven, Belgium; [2]Federal University of Technology - Paraná, Brazil;
[3]Applied Materials, 3050 Bowers Avenue, Santa Clara, CA 95053, USA; [4]Applied Materials, Kapeldreef 75, 3001 Leuven, Belgium.
Tel.: +32-16-28 17 28, Email: Anabela.Veloso@imec.be

Abstract

We report on gate-all-around (GAA) vertically stacked lateral silicon nanosheet (NS) FETs as promising candidates to deliver a better power-performance metric for advanced logic applications for sub-5nm technology nodes *vs.* finFETs. To minimize the parasitic capacitance increase for multiple-sheet structures and enable faster circuits at a given V_{DD}, reduced vertical NS pitch is implemented by using scaled Si/SiGe-multilayer stacks growth. In addition, a novel, thinner gate stack is demonstrated for n-type devices such that it: 1) meets shrinking physical thickness needs; 2) enables tight, low-V_T values, ~105mV smaller than for reference stacks with an Al-based effective workfunction (EWF) metal, with excellent short channel electrostatics control, similar I_G, peak g_m; 3) has improved noise and reliability behavior with uniform N_{ot} *vs.* trap depth profiles and less generation of new defects during stress.

1. Introduction

As conventional, aggressive CMOS scaling is reaching its physical limits with ever more constraining design restrictions, the logic roadmap increasingly faces extra trade-offs between leakage and parasitics *vs.* performance gains. Innovations such as cell height reduction by decreasing the number of metal tracks [1,2] are being pursued to compensate for the more modest pitch scaling, as well as novel device architectures such as GAA nanowire (NW) or NS FETs [2-6] which offer excellent short channel electrostatics control and share many of the finFET fabrication elements. NS FETs have the advantage that they can provide more current per layout footprint thanks to their larger effective widths (W_{eff}), with I_{ON} further boosted by vertically stacking several NS. However, to overcome the capacitance increase for a multiple-sheets structure, features such as inner spacers [2,3,6] and reduction of the vertical distance between the NS [1] are critical to make these devices competitive towards finFETs. To enable obtaining smaller vertical NS pitches, scaled Si/SiGe-multilayers (SiGe as a sacrificial layer for Si NS [2,5,6]) and thinner gate stacks that still meet all the requirements for V_T, leakage, EOT, mobility, variability, noise and reliability are needed. In this work, linked with projected advanced circuits performance and cell layouts, we will demonstrate both these aspects, exploring in detail a novel, scaled gate stack for low-V_T n-type GAA NS FETs with improved device characteristics.

2. Device fabrication

GAA FETs with two vertically stacked Si NS were fabricated using epitaxially grown Si/SiGe-multilayers, in-situ doped epi S/D regions and a dual EWF RMG CMOS flow as described in [2,5]. The NS were formed by selective SiGe removal from the Si/SiGe fins at RMG module and prior to gate stack deposition, a critical step that sets the final NS shape and dimensions [2]. A W fill-metal process finishes the various gate stack sequences evaluated.

3. Results and discussion

Fig. 1 shows a power-performance benchmark calculated for inverter-based ring oscillators (RO) with fan-out of three (FO3) and ~50× contacted-gate-pitch (CGP) length for back-end-of-line load. Beyond the 5nm node (N5), assuming cells with five metal tracks height (Fig. 2) and a change into a one fin per device scenario [1,2,7], additional gains with scaling, at iso-V_{DD}, are compromised for finFET-based cells. At this point, GAA NS FETs are expected to outperform finFETs by delivering faster ROs at a given V_{DD} (e.g., 13% faster at 0.7V, N3) or enabling power savings at matched performance. In addition, improved frequency response can be obtained by reducing the vertical separation between NS to lower the device parasitics (Fig. 1b), with Fig. 2c showing hardware implementation using scaled Si/SiGe-multilayers growth.

Reduced vertical distance between NS requires thinner gate stacks to guarantee similar gate control on all NS surfaces. Starting from the reference n-type gate stack with a 4nm nominal Al-based layer m*, Fig. 3 shows that by considerably thinning down m* (by > 50%) the total physical thickness of the EWF metal stack is substantially and uniformly reduced around all the NS (or NW) surfaces: ~7.5→~4.2nm, though that occurs with a penalty in terms of V_T (V_{Tlin}~0.24→0.6V). Exploring alternative material options, a new, thinner EWF metal n* was introduced in the flow of GAA NS FETs with the results in Fig. 4 confirming that similar small V_T values (V_{Tlin}~0.24-0.26V) are obtained as compared to those for the thicker Al-based reference stack. Moreover, upon the novel stack optimization, further V_T reduction down to V_{Tlin}~0.14V, and also tighter V_T distributions are achieved. In regard to gate leakage (I_G), Fig. 5 shows no significant impact: smaller differences in I_G are measured for devices with the novel n* metal *vs.* NS FETs with the reference, 4nm nominal m* layer than when comparing the latter to thinner m* devices. Similar peak g_m values are extracted for both kinds of gate stack NS FETs which, as displayed by the IV curves in Fig. 6, also exhibit excellent electrostatics control down to short channels. TEM analysis in Fig. 7 shows GAA NS FETs with the optimized n* layer have smaller EWF metal stack physical thickness: ~4.7nm, confirming the successful use of a thinner gate stack in these devices, without compromising DC characteristics.

Overall, Fig. 8 shows improved LF noise behavior for GAA NS FETs with the novel n* EWF metal, with lower normalized input-referred noise spectral density (S_{VG}) values indicating less traps/defects present as compared to the reference stacks. Both types of devices exhibit 1/f noise behavior and, as shown in Fig. 9, proportionality of the normalized current noise spectral density (SI_D/I_D^2) *vs.* $(g_m/I_D)^2$, at lower I_D. This points to carrier number fluctuations as being the dominant mechanism for the LF noise. Moreover, as reported in [8], the EWF metal can have an impact on the oxide trap density (N_{ot}, derived from $S_{VG}.f$ [9]) profile *vs.* trap depth. To illustrate this, Fig. 10 shows the comparison between a sloped *vs.* a considerably uniform profile for GAA NW FETs with TiN *vs.* Al-based EWF metals [4], with similar N_{ot} computed at the Si/SiO_2 interface. Occurrence of oxygen scavenging from the high-*k* layer by Ti, leading to the creation of oxygen defects in the gate stack, is thought to be responsible in this case for the TiN sloped profile. Fig. 11 shows that GAA NS FETs with both the Al-based reference and the thinner, novel n* EWF metals exhibit uniform N_{ot} profiles. Reliability wise, in good agreement with the noise results, Fig. 12 shows improved BTI lifetime is extrapolated for devices with the new n* EWF metal, for which lower ΔN_{eff} and higher PBTI field exponent γ values are also extracted in Fig. 13. These are indicative of an overall better device reliability behavior, corresponding to a narrower distribution of charges/defects in the gate dielectric than for the reference. Lastly, assuming universality of relaxation [10], these defects seem to be mostly pre-existing defects contributing to charge trapping and de-trapping during stress and relaxation as inferred by the larger recoverable (R) *vs.* permanent (P) BTI degradation components in Fig. 14. In addition, a less steep P *vs.* t_{stress} slope indicates there is also less generation of new defects during stress for the novel n*-based GAA NS FETs.

4. Conclusions

GAA vertically stacked Si NS FETs with reduced vertical distance between sheets are enabled by scaled Si/SiGe-multilayers growth, with a novel, thinner gate stack demonstrated to yield tight, low-V_T values (<0.2V - NMOS), improved noise and reliability behavior, and excellent short channel device characteristics.

References

[1] M. Garcia Bardon *et al.*, IEDM *Tech. Dig.* (2016) 687; [2] H. Mertens *et al.*, IEDM *Tech. Dig.* (2017) 828; [3] S.-G. Hur *et al.*, IEDM *Tech. Dig.* (2013) 649; [4] A. Veloso *et al.*, VLSI *Tech. Dig.* (2015) 138; [5] H. Mertens *et al.*, IEDM *Tech. Dig.* (2016) 524; [6] N. Loubet *et al.*, VLSI *Tech. Dig.* (2017) 230; [7] S. C. Song *et al.*, VLSI *Tech. Dig.* (2015) 198; [8] W. Fang *et al.*, IEEE Elect. Dev. Lett. **37** (2016) 363; [9] E. Simoen *et al.*, ECS J. Solid State Sc. and Tech. **3** (2014) Q127; [10] B. Kaczer *et al.*, IRPS *Tech. Dig.* (2008) 20.

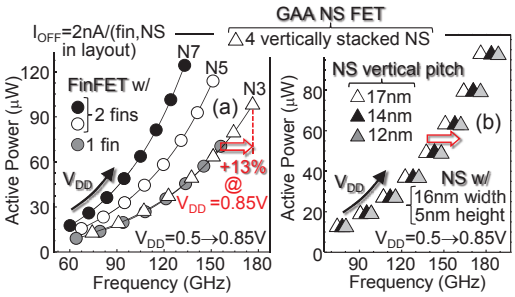

Fig.1 – Simulated power-performance benchmark for ring oscillators. CGP/metal-pitch (MP) values of 56/40 → 48/28 → 45/21 (dimensions in nanometers) were assumed for the nodes N7 → N5 → N3, respectively. a) shows that GAA NS FETs are projected to outperform finFETs at N3 by delivering faster ROs at a given V_{DD}, while (b) illustrates that their speed can be further improved by reducing the vertical distance between the stacked NS to minimize the device parasitics.

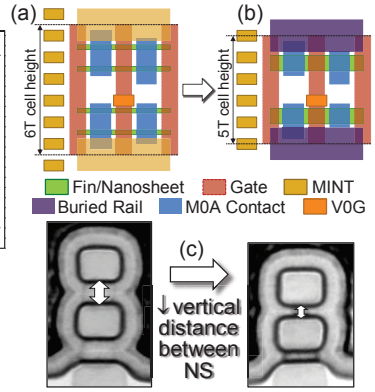

Fig.2 – a,b) show standard cell layouts with 6 or 5 metal tracks (T) cell height. The latter consists of one NS in the floor plan per transistor, corresponding to the NS FETs used in Fig.1 at N3. c) shows reduced NS vertical pitch implementation.

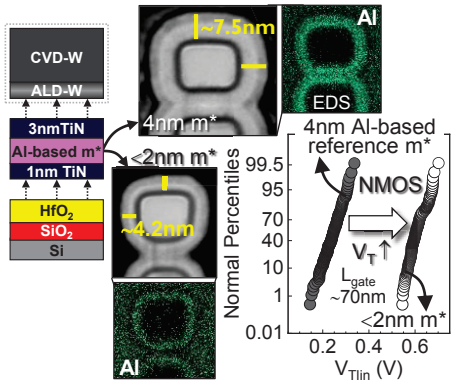

Fig.3 – For Al-based reference n-type GAA FETs, scaling of the EWF metal thickness is confirmed feasible by physical analysis (e.g., TEM, EDS) upon deposition of a thinner Al-based layer (m*), though at the expense of an increase in V_T (data for >50% m* thickness reduction shown here).

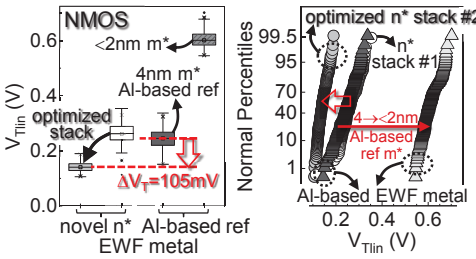

Fig.4 – Smaller V_{Tlin} values and tighter V_{Tlin} distributions are achieved for n-type GAA NS FETs using an optimized gate stack with a new EWF metal layer n* as compared to reference Al-based devices (data for L_{gate}~70nm shown here).

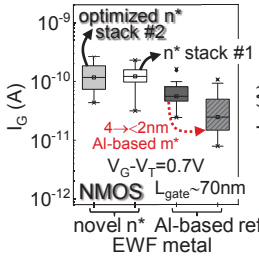

Fig.5 – Smaller differences in I_G are measured for GAA NS FETs with the 4nm Al-based reference layer m* *vs.* the novel EWF metal n* than when using a thinner m*.

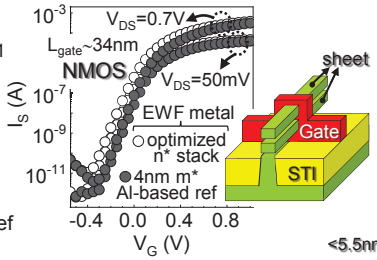

Fig.6 – Excellent electrostatics (e.g., SS~68-72mV/dec) and similar peak g_m values are measured for GAA NS FETs with the 4nm Al-based reference EWF metal or the optimized n* gate stack.

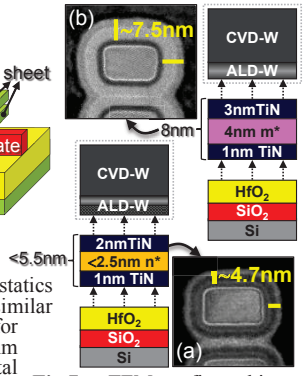

Fig.7 – TEM confirms thinner gate stacks (~3nm smaller) are obtained with the novel n* EWF metal (a) *vs.* the 4nm Al-based reference process m* (b) (layer nominal thicknesses in the schematics, with verified n* physical thickness <2.5nm).

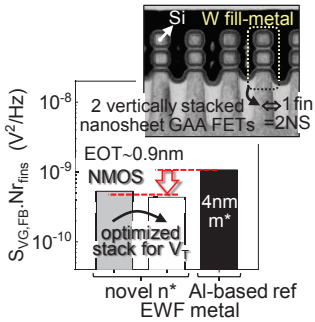

Fig.8 – Slightly improved LF noise values are measured for GAA NS FETs (with two vertically stacked nanosheets) built using the novel, thinner n* EWF metal *vs.* reference devices with the 4nm Al-based layer m* in the gate stack.

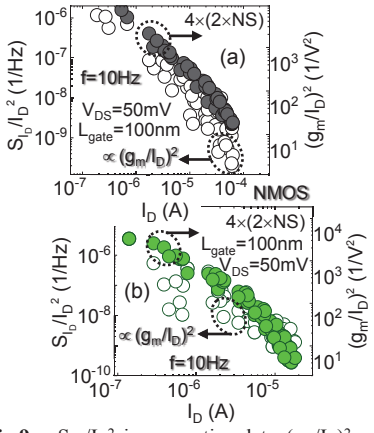

Fig.9 – S_{ID}/I_D^2 is proportional to $(g_m/I_D)^2$, at lower I_D, for both: (a) 4nm Al-based m* reference, and (b) new, thinner n* EWF metal stacks. The dominant mechanism for the LF noise is thus similar for both types of devices.

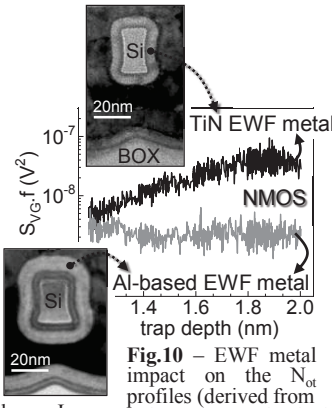

Fig.10 – EWF metal impact on the N_{ot} profiles (derived from S_{VG}.f) *vs.* trap depth in GAA NW FETs: sloped (and with N_{ot} increasing towards the metal gate) for the TiN, uniform for the Al-based devices in [4].

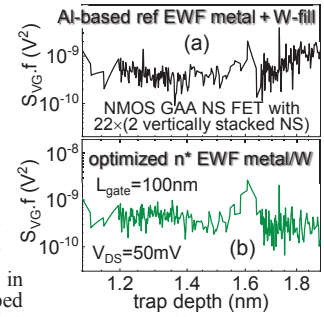

Fig.11 – Uniform N_{ot} *vs.* trap depth profiles are extracted for GAA NS FETs with: (a) Al-based reference stack, or (b) new, thinner EWF metal.

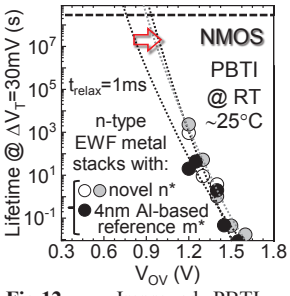

Fig.12 – Improved PBTI lifetime is extracted for GAA NS FETs with two vertically stacked nanosheets and built using the novel, thinner n* EWF metal as opposed to the 4nm Al-based m* reference gate stack process.

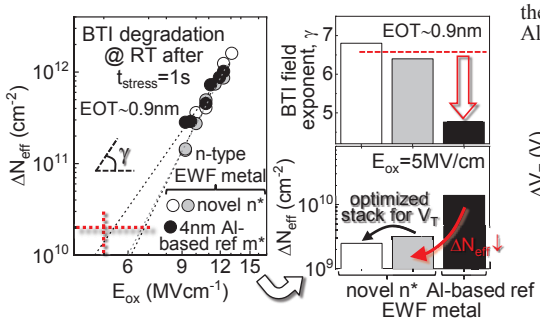

Fig.13 – Lower ΔN_{eff} and higher γ values are measured for NS FETs with the novel, thinner n*-based gate stacks. They are indicative of better reliability, with a narrower distribution of charges/defects in the gate dielectric *vs.* the Al-based reference.

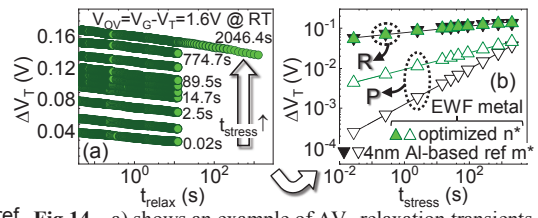

Fig.14 – a) shows an example of ΔV_T relaxation transients after increasing the stress time (t_{stress}) for GAA NS FETs with the novel, thinner n* EWF metal. These devices also show in (b) a less steep slope for the permanent (P) BTI degradation component *vs.* t_{stress}, indicating generation of less new defects during stress than the Al-based reference.