Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp561-562

Statistical Analysis of Temperature Dependence of Worst Case SRAM Data Retention Voltage Using Extreme Value Theory

Tomoko Mizutani, Kiyoshi Takeuchi, Takuya Saraya, Masaharu Kobayashi and Toshiro Hiramoto
Institute of Industrial Science, The University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan
Phone: +81-3-5452-6264, E-mail: mizutani@nano.iis.u-tokyo.ac.jp

Abstract

The worst case data retention voltage (DRV) in bulk and SOTB SRAM was statistically analyzed using the extreme value theory. It was confirmed that the worst case DRV follows a Gumbel distribution. By extrapolating the fitted Gumbel distribution, the worst case DRV of large capacity SRAM at high temperature is estimated.

1. Introduction

Due to random characteristics variability of transistors, some SRAM cells fail at very low supply voltage (V_{DD}) and the minimum operation voltage of an SRAM chip or macro is determined by the worst case cell [1]. The cell stability of the worst case cell can be estimated by the statistical distribution of the stability metric of all cells. However, it is not realistic to measure the stability metrics of all the cells.

In previous study [2], we statistically analyzed DRV of the worst case bulk SRAM cells by the extreme value theory [3-6] and found that worst case DRV follows the Gumbel distribution. In this study, we extended the analysis method to silicon-on-thin-box (SOTB) SRAM. Furthermore, the temperature dependence of DRV in bulk and SOTB SRAMs were evaluated and the worst case DRV at higher temperature was estimated.

2. Measurement

The DRV values of 16k bulk and SOTB SRAM cells were measured one by one at 25°C, 60°C, and 100°C using 6T-SRAM DMA-TEG with the 65 nm technology [7]. V_{DD} was swept under the voltage conditions shown in Fig.1, monitoring the voltages at internal nodes VL and VR. DRV is determined as the V_{DD} voltage at which the high-side and the low-side voltage switch [8]. Fig.2 shows the normal quantile plots of measured threshold voltages (V_{TH}) of cell transistors, confirming that V_{TH} of nFETs and pFETs of bulk and SOTB SRAMs are almost the same at room temperature and that SOTB SRAM has smaller V_{TH} variability. Both average V_{TH} and V_{TH} variability decrease at high temperature. SOTB transistors have larger temperature dependence. The reason may be related to degraded short channel effect in bulk transistors [9]. The temperature dependence is not the same in nFETs and pFETs.

Fig.3 shows the normal quantile plots of measured DRV of 16k bulk and 16k SOTB SRAM cells. DRV is not normally distributed, so it is difficult to estimate the worst case value at the right heavy tail. Bulk DRV fluctuates more than SOTB DRV due to larger V_{TH} variability. As the temperature rises, DRV increases. In order to apply the extreme value theory, 16k measured DRV data were divided into 64 blocks, each containing 256 DRV data, and the maximum (worst case) DRV in each block was extracted.

3. Results and Discussion

According to the extreme value theory (Fig.4), the distribution function G of the maximum value of n independent and identically distributed random variables converges to Weibull ($\xi<0$), Gumbel ($\xi=0$), or Fréchet distribution ($\xi>0$) depending on the sign of the shape parameter ξ. We reported that the worst case bulk DRV is fitted to a Gumbel distribution [2]. Fig.5 shows the Gumbel quantile plots of the measured worst case DRV in bulk and SOTB SRAM cells. All plots are approximately straight, confirming that the worst case bulk DRV as well as SOTB DRV at all temperatures are fitted to a Gumbel distribution.

The worst case DRV of larger capacity SRAMs can be estimated by extrapolating the fitted Gumbel distribution function (Fig.6). Fig.7 shows the extrapolated worst case DRV as a function of the number of blocks. The 95% confidence intervals calculated using the delta method [3,4] are also shown by shades. It is found that (i) the difference between 25°C and 100°C is larger in SOTB SRAM and (ii) the two extrapolation curves approach and the temperature dependence diminishes in bulk SRAMs as the capacity increases. (i) is explained by the fact that SOTB transistors have larger temperature dependence and nFET and pFET have different temperature dependences (Fig.2). The cell transistors operate in the subthreshold region around DRV and the cell stability is very sensitive to slight parameter changes in SOTB SRAMs. As a result, the DRV degradation is larger at higher temperature in SOTB SRAM. (ii) may be related to smaller V_{TH} variability at high temperature in bulk transistors (Fig.2) but is not simply explained, calling for further analysis.

4. Conclusions

The worst case DRV of bulk and SOTB SRAMs are analyzed statistically using the extreme value theory and the worst case DRV of large capacity SRAM at high temperature is estimated. It is estimated that the temperature dependence of DRV becomes week in bulk SRAM as the SRAM capacity increases.

References

[1] H. Qin et al., ISQED, (2004) 55.
[2] T. Mizutani et al., to be presented in Si Nano Workshop, 2019.
[3] S. Coles, "An Introduction to Statistical Modeling of Extreme Values," Springer, (2001).
[4] R. Takahashi and T. Shimura, "Extreme Value Statistics (in Japanese)", Kindai-Kagaku-sha, (2016).
[5] E. Gilleland and R. W. Katz, JSS **72** (2016) 1.
[6] R. L. Smith, Biometrika **72** (1985) 67.
[7] Y. Yamamoto et al., VLSI Tech. Dig., (2013) 212.
[8] T. Mizutani et al., Jpn. J. Appl. Phys. **57** (2018) 04FD08.
[9] S. Gao, unpublished.

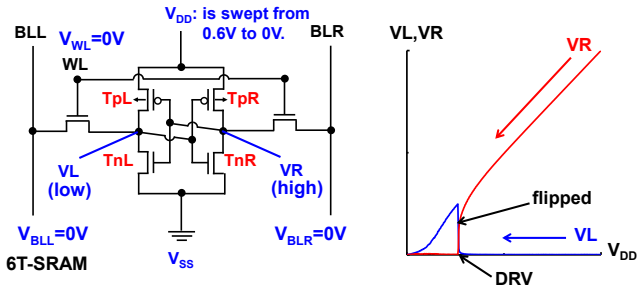

Fig.1. Schematics of a 6T-SRAM cell and the method of DRV measurement. In this example, VL node is low and VR node is high. V_{DD} is scanned from 0.6V to 0V. The same operation is done for VR=low.

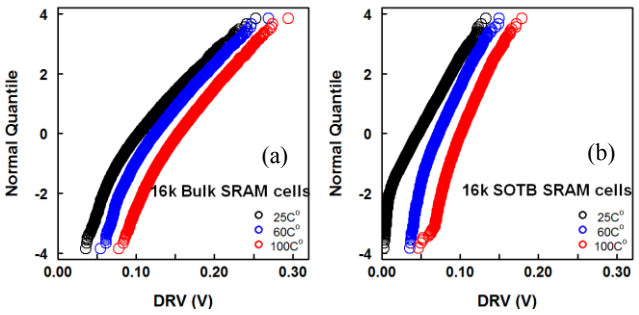

Fig.3. Normal quantile plots of measured DRV of (a) 16k bulk and (b) 16k SOTB SRAM cells at various temperatures.

Original random variable: X_i

$$P(X_i \le z) = F(z)$$

Worst case random variable: $M_n := \max\{X_1, X_2, \cdots, X_n\}$

$$P(M_n \le z) = \{F(z)\}^n.$$

Suppose $a_n(>0), b_n \in \mathbb{R}$ exist such that

(Basic assumption) $P\{(M_n - b_n)/a_n \le z\} \to G(z)$ as $n \to \infty$,

then $\sigma(>0), \mu \in \mathbb{R}$ exist for enough large n such that

$$G(z) = \exp\left[-\left\{1+\xi\left(\frac{z-\mu}{\sigma}\right)\right\}_+^{-1/\xi}\right], \quad (1)$$

where $y_+ := \max\{y, 0\}$, $\sigma > 0$. If $\xi = 0$ (Gumbel case),

$$G(z) = \exp\left[-\exp\left\{-\left(\frac{z-\mu}{\sigma}\right)\right\}\right], \quad (2)$$

Fig.4. Summary of the extreme value theory [3,4].

Estimates of extreme quantiles of a Gumbel distribution are obtained by inverting Eq.(2)

$$z_p = G^{-1}(1-p) = \mu - \sigma\log\{-\log(1-p)\}, \quad (3)$$

where p is the upper tail probability.

The mean

$\mu + \sigma\gamma$, γ: the Euler-Mascheroni constant

and the standard deviation

$$\sigma\frac{\pi}{\sqrt{6}},$$

for the Gumbel distribution are calculated, where σ is the scale parameter of the Gumbel distribution

Fig.6. Estimates of extreme quantiles of a Gumbel distribution by the extreme value theory [3,4]. The mean and the standard deviation also can be obtained.

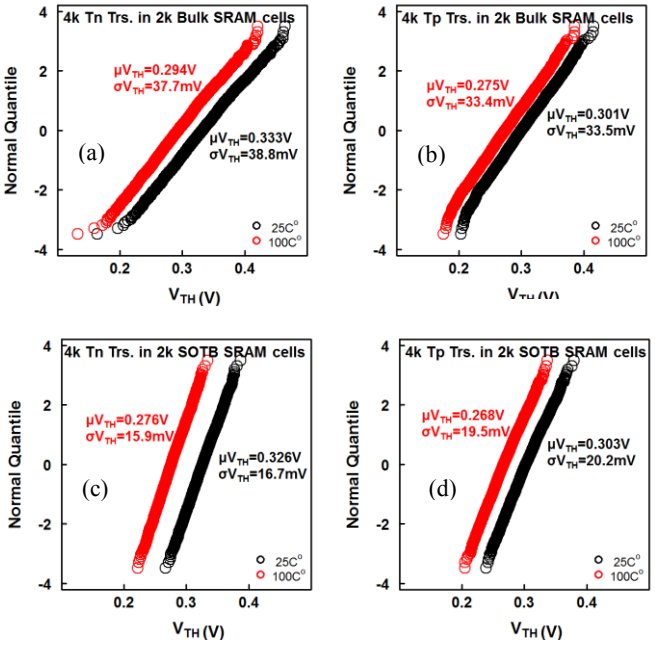

Fig.2. Normal quantile plots of measured V_{TH} of 4k cell transistors in 2k SRAM. (a) nFETs and (b) pFETs of bulk SRAM cells, (c) nFETs and (d) pFETs of SOTB SRAM cells.

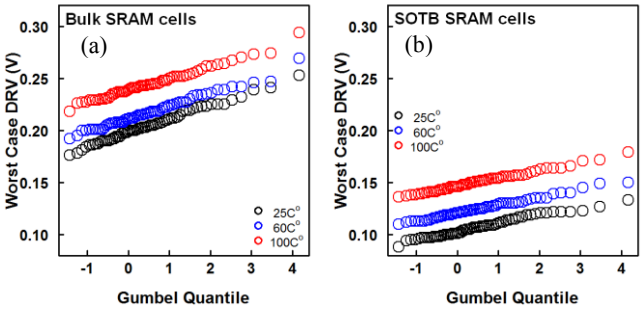

Fig.5. Gumbel quantile plots of the measured worst case DRV in (a) bulk and (b) SOTB SRAM cells at various temperatures.

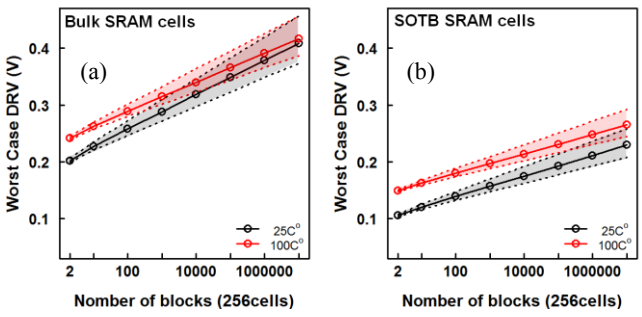

Fig.7. The extrapolated worst case DRV as a function of the number of blocks. The worst case DRV corresponds of a cumulative probability of 1/(number of blocks). The 95% confidence intervals by the delta method are also taken into account. (a) Bulk and (b) SOTB SRAM cells.