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Evaluation of 2D Negative-Capacitance FET Based Subsystem-Level Logic Circuits Considering Ferroelectric Nonuniformity

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Abstract

This work evaluates the circuit performance of 2D MFIS-type negative-capacitance FETs (2D-NCFETs) based on the IRDS 2030 node considering the ferroelectric nonuniformity. With the aid of a scalable short-channel 2D-NCFET compact model, the functionality and performance of static and dynamic logic circuits such as the 4-bit Manchester carry-chain (MCC) adder have been investigated. Our study indicates that, in addition to the improvement of subthreshold slope, the reduced V_{ds} dependence of threshold voltage and the suppressed body effect of the NCFET also contribute to the performance improvement especially for the pass-transistor logic (PTL). However, the nonuniformity in the ferroelectric thickness (T_{FE}) may significantly degrade the performance of logic circuits using NCFETs.

1. Introduction

With a ferroelectric insulator compatible with state-of-the-art CMOS gate stack, the negative-capacitance FET (NCFET) [1] with steep subthreshold slope has garnered substantial interest and has been considered as a promising device candidate for future low-power applications. In order to achieve better short-channel control for meeting the requirement of future technology nodes, 2D transition-metal-dichalcogenides (TMDs), such as MoS_2 and WSe_2 are very attractive channel materials for NCFETs [2] due to their atomically-thin thickness and adequate bandgap. Recently, the first short-channel top-gated 2D-FET fabricated on SiO_x/Si substrate using metal-assisted CVD with impressive electric characteristics has been demonstrated [3]. However, it has been reported that the ferroelectric film can be non-uniform in thickness, leading to varying ferroelectric properties [4]. How might the ferroelectric nonuniformity affect the circuit performance has rarely been known and merits investigation. In this work, we investigate the performance of 2D-NCFET based static and dynamic logic circuits and consider the impact of the T_{FE} variation using Monte-Carlo simulation.

2. Methodology

Fig. 1 shows the schematic of the MFIS-type 2D-NCFET used in this study. An accurate and physical short-channel MFIS-type model [7][8] is adopted to evaluate the performance of 2D-NCFET based logic circuits. The channel length used in this work, Lg=10nm, is based on the IRDS 2030 node, and the 2D-FETs and 2D-NCFETs are designed to possess equal $I_{OFF,Sat}$ =30pA/μm as shown in **Fig. 2**. The ferroelectric parameters used in this work are based on the data in [5]. Pertinent parameters of channel materials for monolayer MoS_2 and WSe_2 are listed in **Table1.** Baseline 2D-FET parameters are extracted from numerical TCAD simulation. In order to model the impact of drain-coupling on the NC effect, physical modeling of the subthreshold swing (SS) and V_T shift based on a scalable short-channel polarization charge model are included to capture distinct short-channel effects such as the reduced DIBL of the NCFET as shown in **Fig. 2**. The nonuniformity in T_{FE} may degrade ferroelectricity and increase the dielectric (DE) layer thickness simultaneously, which further increases EOT and exacerbates the circuit performance. Using Monte-Carlo simulations, in this work, the nominal T_{FE} value is set to be 75% of the ideal case with 3σ tolerance up to 25% as illustrated in **Fig. 7** to evaluate the impact of the ferroelectric nonuniformity on circuit performance**.**

3. Results and Discussion

Fig. 3 shows the comparison of delay improvement for both static logic circuits (5-stage inverter and transmission-gates) and the dynamic MCC adder (with the functionality demonstrated in **Fig. 4**). We further dissect the delay improvement for 5-stage inverter and transmission gates at V_{DD}=0.4V in **Fig. 5**. Apart from the benefit of SS improvement due to the NC effect, the reduced V_{ds}-dependency of V_T and the suppressed body effect of NCFETs also play a crucial role for the performance especially for the PTL operating at lower V_{DD}. The suppressed body effect can be elucidated by the following V_T expression of the NCFET:

$$V_{T,NCFET} = V_{T,2D\text{-}FET} + 2\alpha T_{FE} Q_{int} + 4\beta T_{FE} Q_{int}^3$$

Different from inverters with body and source terminal always connecting together, PTLs suffer from inherent reverse Vbs effect during switching. Since the body terminal of PTLs is grounded and the source voltage varies with the input signal, the V_T of the underlying 2D-FET is increased. However, for NCFETs, the internal polarization charge (Q_{int}) also increases with the reverse Vbs which mitigates the increasing V_T. This further explains why transmission-gates and the MCC adder exhibit larger delay improvement compared to inverters. If the internal voltage gain of NCFETs becomes larger, negative body-effect coefficient can be expected as shown in **Fig. 6.**

From Monte-Carlo simulation, **Fig. 8** shows the average delay distributions of logic circuits considering the T_{FE} nonuniformity. It is worth noting that, albeit the switching delays of ideal logic circuits using NCFETs exhibit substantial improvement, they become comparable or even worse than the baseline 2D-FET counterparts when taking the T_{FE} variation into consideration.

Acknowledgements

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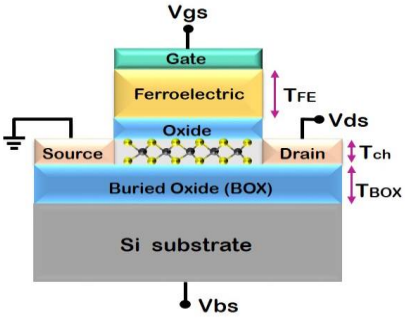


Fig. 1. Schematic of a MFIS-type 2D-NCFET (MoS_2-n, WSe_2-p) with channel thickness (T_{ch}) =0.65nm, EOT=0.65nm and BOX thickness (T_{BOX})=5nm

Table.1. Pertinent parameters of the channel material (MoS_2-n, WSe_2-p) used in this paper. [6]

Parameters	Monolayer MoS_2 (NMOS)	Monolayer WSe_2 (PMOS)
Band-gap [eV]	1.67	1.542
Electron affinity [eV]	4.28	3.61
Dielectric constant	4.8	4.5
Effective mass [m_0]	m_e=0.467	m_e=0.364
	m_h=0.544	m_h=0.344

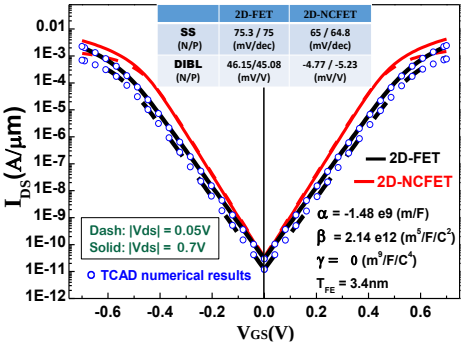


Fig. 2. Hysteresis-free I_{ds}-V_{gs} characteristics of the simulated 2D-FETs and 2D-NCFETs with equal $I_{OFF,Sat}$. Reduced DIBL for the NCFET can be seen

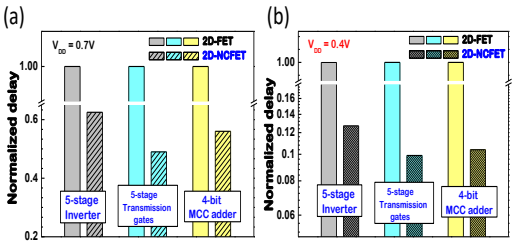
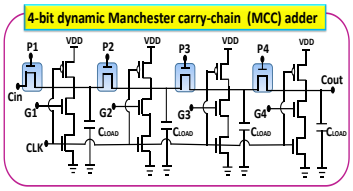


Fig. 3. Comparison of delay improvement in 5-stage inverter, transmission-gates and dynamic MCC adder using 2D-NCFETs. The transmission gates and MCC adder exhibit larger delay improvement than the inverter counterpart.



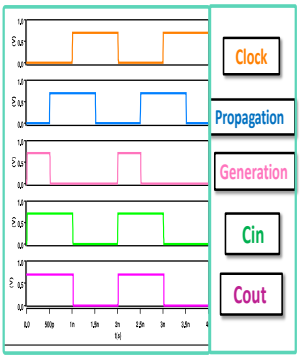


Fig.4. Schematic and functionality of the dynamic 4-bit MCC adder with 2D-NCFETs. Note the NMOS pass-gate elements in the critical path of the MCC adder.

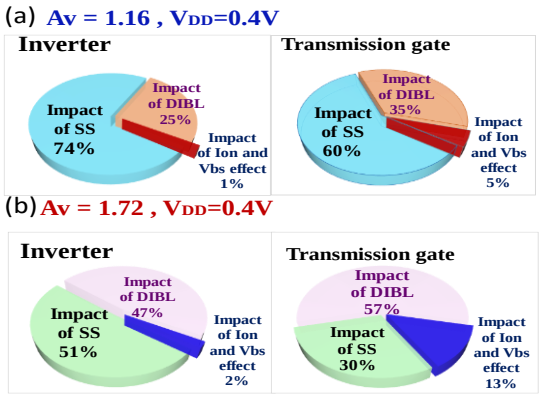


Fig. 5. Dissection of delay improvement for 5-stage inverter and transmission gate using 2D-NCFETs with (a) Av=1.16 and (b) Av=1.72

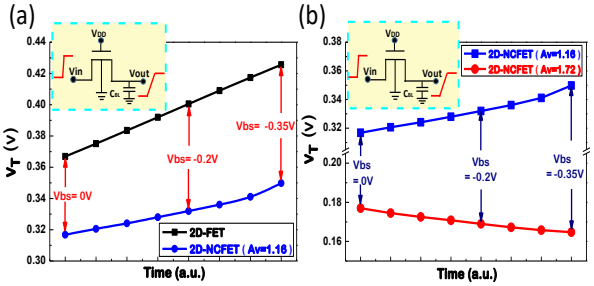


Fig. 6. Comparison of time dependence in V_T between (a) 2D-FET versus 2D-NCFET with Av=1.16 and (b) 2D-NCFET with Av=1.16 and 1.72 during switching in the NMOS pass gate.

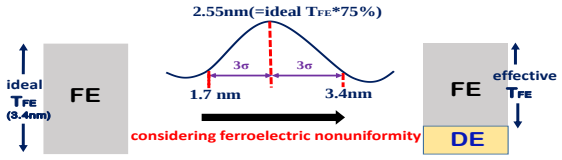


Fig. 7. Method of the Monte-Carlo simulation considering the ferroelectric nonuniformity.

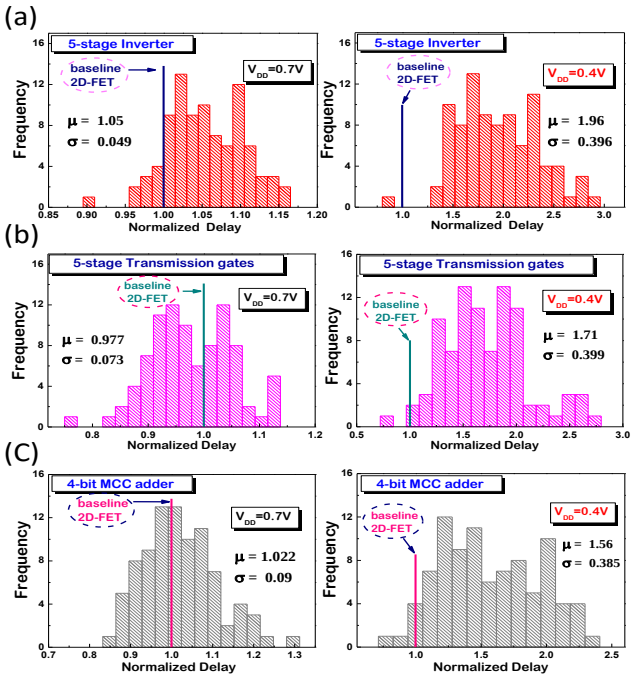


Fig. 8. Delay distributions for (a) 5-stage inverters (b) 5-stage transmission gates and (c) 4-bit MCC adder with 2D-NCFETs at V_{DD}=0.7V & 0.4V using Monte-Carlo simulation. The mean value and sigma of delay are normalized to baseline 2D-FETs.