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Impact of Channel Flattening Process on Device Performance of Ge *n*MOSFETs with Different Surface Orientations

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Abstract

The impact of channel flattening process, dozen digital etching (DDE), on device performance of Ge nMOSFETs with different surface orientations of (100), (110), and (111) has been investigated. 20 times DDE was found effective for improving electron mobility, especially for (100) surface. Decrease of interfacial trap density and reduction of surface roughness owing to DDE could explain these phenomena. Orientation/flatness-dependent performance should be an important concern for future Ge 3D devices, such as FinFETs and nano-wire/sheet FETs.

1. Introduction

Recent evolution of Ge FETs architecture demands morphological channel engineering utilizing the heterogeneity of crystal orientation. High performance FinFETs [1], ultrathin body (UTB) FETs [2] and gate-all-round (GAA)FETs [3] with various channel surfaces have been demonstrated so far. It is known that Ge surface orientation and its flatness can greatly impact its carrier mobility [4-6]. Therefore, the optimization of surface orientation/channel direction with extremely flat surfaces are of great importance for future Ge 3D devices. Recently, we have successfully demonstrated ultra-smooth GeOI UTB channels with enhanced device performance [6] by utilizing dozens digital etching (DDE), which is cyclic process of plasma oxidation and wet etching at room temperature. DDE should also be useful for fabricating Ge 3D channels because of its precise channel thickness controllability and effectiveness for surface roughness smoothening without thermal stress as shown in Fig. 1. In this work, flattened Ge surfaces of (100), (110) and (111) orientation were attained by DDE and the impact of flatness, surface orientation on device performance has been systematically investigated.

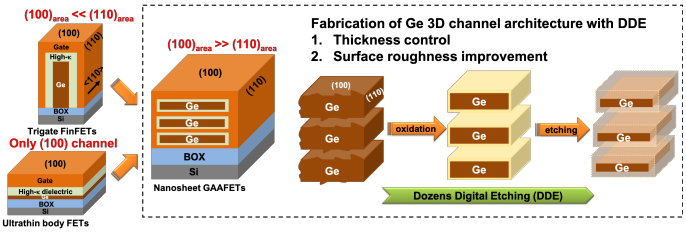

Fig. 1 Evolution of Ge 3D device architecture utilizing different surface orientations with varied area ratio. DDE process is promising technology for fabricating Ge 3D channel structures because of its excellent thickness controllability and remarkable surface flattening effect.

2. Experimental

p-type Ge (100), (110), and (111) wafers with resistivity of 0.2-0.8 Ω-cm were used for fabricating bulk Ge *n*MOSFETs. Fig. 2 shows the surface morphology of (100) surface before and after 20 times DDE. Significant improvement of surface roughness has been observed after DDE. Fig. 3 shows the DDE cycles dependence of etching depth and RMS surface roughness of (100), (110), and (111) surfaces. The DDE rate with different surface orientations were almost the same, while the effect of reducing surface roughness was more profound on (100) surface. Different cycles of DDE (0/10/20 cycles) were performed on Ge (100), (110) and (111) wafers just before the ALD-Al_2O_3 deposition. The detailed device fabrication process can be found elsewhere [7].

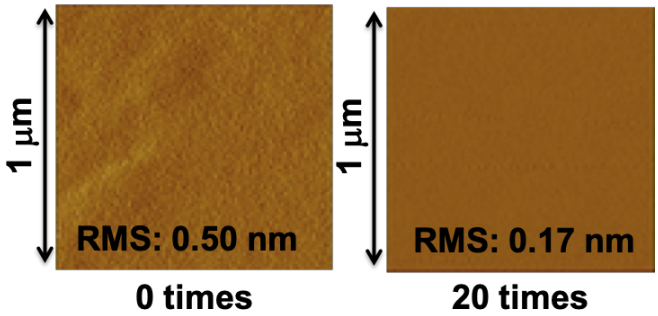

Fig. 2 Surface morphology of (100) surface before (left) and after (right) 20-cycle DDE characterized by AFM.

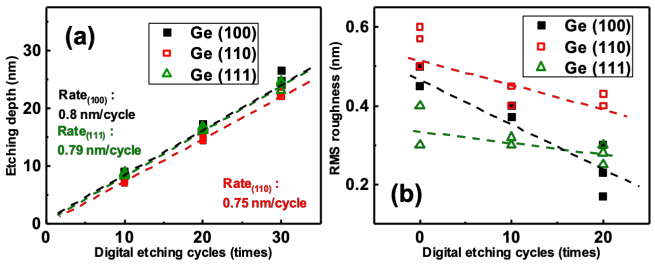

Fig. 3 DDE cycle dependence of (a) etching depth and (b) RMS surface roughness of (100), (110) and (111) surfaces extracted from AFM.

3. Result and Discussion

The transfer curves of (100), (110), and (111) *n*MOSFETs with 1 μm gate length fabricated with and without 20 times DDE are shown in Fig. 4. Higher maximum I_D were observed on (100), (110), and (111) after 20 times DDE, indicating the effectiveness of DDE

on improving device performance of Ge *n*MOSFETs even with different surface orientations. The DDE cycles dependences of subthreshold slope (S.S.) for (100), (110), and (111) *n*MOSFETs is shown in Fig. 5. Higher S.S. on (110) surface indicated higher D_{it} at Al_2O_3/Ge (110) interface. For both (100) and (110), no distinct change of S.S. by DDE was observed, indicating that DDE does not affect initial MOS interface quality. On the other hand, DDE was found to be effective in lowering D_{it} at Al_2O_3/Ge (111) interface, as the S.S. significantly decreased from ~120 to ~80 mV/dec. after 20 times DDE.

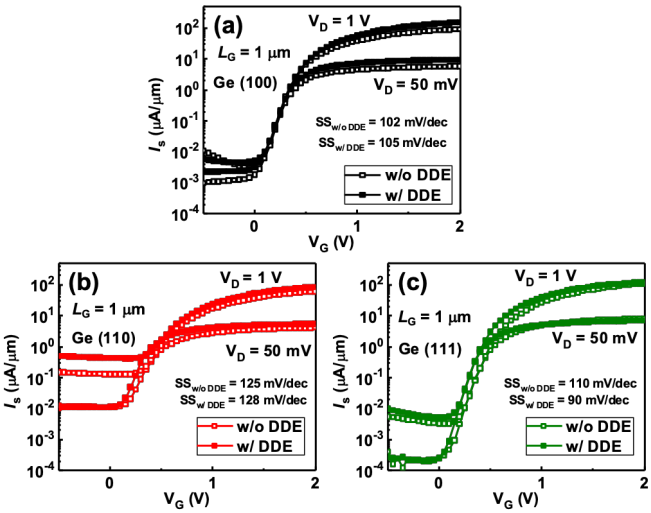

Fig. 4 Transfer curves of (a) (100) (b) (110) and (c) (111) Ge *n*MOSFETs fabricated with and without 20 times DDE process. S.S. value before and after 20 times DDE were also shown.

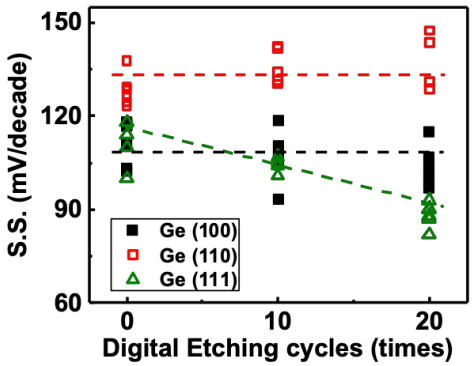

Fig. 5 DDE cycle dependence of S.S. of (100), (110) and (111) Ge *n*MOSFETs.

The transconductance curves extracted at V_D of 1 V for (100), (110), and (111) *n*MOSFETs with and without DDE are shown in Fig. 6. Enhancement of peak transconductance was observed clearly with different surface orientation, suggesting the improvement of field effect mobility after DDE. Compared with (110) and (111), (100) devices showed the most significant improvement of mobility, which can be attributed to the effect of surface flattening of DDE as shown in Fig. 3(b). Suppression of Coulomb scattering was also expected for (111) device as the interfacial trap density decreased after DDE. By using the following formula: $\mu_{FE} = L_G \cdot G_m/W \cdot C_{ox} \cdot |V_D|$, we summarized the DDE cycles dependence of field effect mobility for (100), (110), and (111) *n*MOSFETs in Fig. 7. It is found that DDE was effective for mobility enhancement, especially for those on Ge (100). About 1.5 times mobility enhancement was attained for (100) devices after 20 times DDE process.

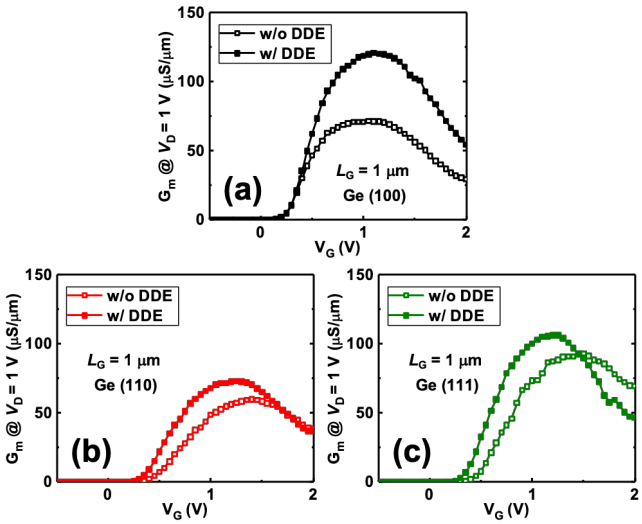

Fig. 6 Transconductance curves of (a) (100) (b) (110) and (c) (111) Ge *n*MOSFETs fabricated with and without 20 times DDE. S.S. value before and after 20 times DDE.

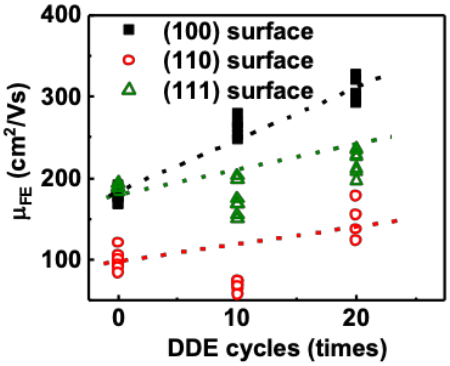

Fig. 7 DDE cycle dependence of field effect mobility of (100), (110) and (111) Ge *n*MOSFETs.

4. Conclusion

Improvement of electron mobility were attained on Ge *n*MOSFETs especially for (100) surface orientation after DDE thanks to the surface flattening effect. Considering the device performance with different surface orientation, Ge 3D channel structures with proper surface flattening process are favorable for future FinFETs and nano-wire/sheet FETs.

Acknowledgement

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Reference

[1] J. Feng et al., *EDL* **28**, 637 (2007). [2] W. H. Chang et al, *VLSI* 192 (2017). [3] C. L. Chu et al., *EDL* **39**, 1133 (2018). [4] C. H. Lee et al, *IEDM* 416 (2010). [5] R. Zhang et al., *IEDM* 326 (2016). [6] W. H. Chang et al, *VLSI* 191 (2018). [7] W. H. Chang et al., *EDL* 37, 253 (2016).