## **3D-stacked Highly Strained SiGe/Ge Gate-All-Around (GAA) pFETs** Fabricated by **3D Ge Condensation**

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Abstract: This paper reports on 3D stacking of highly strained SiGe/Ge GAA pFETs fabricated by 3D Ge condensation. Our proposed method is highly stackable with either nanosheet (NS) or nanowire (NW) channels and does not require strain relaxed buffers (SRB) to incorporate strain in channels. 3D Ge condensation of suspended channels enables achieving uniaxial compressive strain of ~2.5%, confirmed by diffraction pattern using scanning transmission electron microscopy (STEM). Through the geometric optimization of channels, compressive strain can be effectively increased with less buckling, resulting in the suppression of undesirable hole generation. As a result, high hole mobility ( $\mu$ ) of 617 cm<sup>2</sup>/Vs is demonstrated.

**Introduction:** Incorporating high mobility material in channel and 3D stacking channels in a multigate/surroundgate device can enable next-generation high-performance CMOS technology [1,2]. Ge is a potential channel material due to its superior  $\mu$  and light effective mass. Also, Ge condensation is an appealing technique to introduce strained Ge (s-Ge) onto Si platform without SRB as a result of its excellent compatibility with Si technology and, more importantly, the ease of controlling critical dimension (CD) [3]. However, the conventional Ge condensation on SOI does not allow 3D stacking of channels and shows a large degree of strain relaxation [3,4]. We propose a novel method with high stackability to fabricate 3D-stacked strained SiGe/Ge GAA device architecture with large uniaxial compressive strain by 3D Ge condensation.

3D stacking of strained SiGe/Ge by 3D Ge condensation Fig. 1a displays the schematic of our 3D-stacked Ge GAA structure and Fig. 1b shows a scanning electron microscopy (SEM) image of the structure. High quality pseudomorphic SiGe multilayers are grown on Si and patterned. The SiGe channels are released by tetramethylammonium hydroxide (TMAH), followed by Ge condensation [3] all around the channels (3D) to achieve Ge-rich SiGe or pure Ge. It should be pointed out that the suspended Si<sub>0.7</sub>Ge<sub>0.3</sub> becomes Ge-rich SiGe as Ge condensation proceeds while S/D remain Si-rich SiGe, which allows our structure to be highly compatible with the incumbent Si contact technology, especially for nFETs. It is confirmed by X-ray diffraction (XRD) that the peak of the initial Si<sub>0.7</sub>Ge<sub>0.3</sub> is split into two in which one approaches Ge peak and the other one (S/D) moves towards Si peak (Fig. 3). Raman spectra are taken over the course of 3D Ge condensation (Fig. 4) to determine Ge composition and strain [5]. Fig. 5 shows Raman spectral imagining of Ge-Ge mode along with the SEM image of 3D-stacked GAA, which supports the idea that Ge enrichment takes place only in the channel, consistent with Fig. 3. NS and NW configurations (Fig. 6) can be made by proper sizing of initial SiGe and fin width before the channel release. High quality of single crystalline Ge NW is captured by TEM (Fig. 7).

## 4D-STEM strain mapping of stacked NWs

Buckling of long NWs (high aspect ratio (AR)) caused by Ge condensation induced compression is observed in Fig. 8. To further understand this, 4D-STEM strain mapping is used to measure strain distribution in 200nm and 500nm long Si0.25Ge0.75 NWs. To ensure accuracy, line scans from the Si bulk through the centers of each NW are performed: NW diffraction patterns are compared to those of the Si bulk. Fig. 9a reveals the uniaxial compressive strain for the 500nm long NWs along its length to be  $\sim 1.2\%$  (line scan along the NW length is also shown). In contrast, Fig. 9b shows compressive strain for the 200nm long NWs along their length to be  $\sim 2.5\%$ . Accommodation of the higher compressive strain in the shorter NWs (small AR) is supported by the observation of increased buckling in longer NWs (Fig. 8), consistent with strain relaxation being limited by the smaller AR of the NWs. Therefore, through the geometric optimization of GAA channels, it is possible to achieve high compressive strain, which benefits the performance of pFETs [1,3,4].

## Highly strained SiGe/Ge GAA pFETs

To examine the electrical characteristics, 3-stacked s-SiGe GAA pFETs are fabricated with 10nm Al<sub>2</sub>O<sub>3</sub>/25nm TiN gate stack [6] and metal S/D. Fig. 10a shows ID-VGs characteristics with 60% and 75% Ge. It should be pointed out that V<sub>th</sub> does not shift positively with higher Ge %, indicative of high quality channels produced by our method without a significant amount of undesirable hole generation by crystal defects [4]. I<sub>D</sub>-V<sub>DS</sub> is shown in Fig. 10b, demonstrating that 3D stacking enables the high drivability of the pFETs in a limited footprint. Fig. 11a shows Vext shift (Vext: Intercept at VGS axis of linear extrapolation of I<sub>D</sub>-V<sub>GS</sub> at g<sub>m</sub> max.) with respect to Vext at NW length (L<sub>NW</sub>)=200nm as a function of L<sub>NW</sub>. It should be highlighted that more positive V<sub>ext</sub> shifts are observed at the longer NWs (high AR), attributable to defect induced hole generation through buckling, consistent with Fig. 8. High hole mobility of 617 cm<sup>2</sup>/Vs (Fig. 11b), extracted by Y-function, is achieved, ascribed to high Ge % combined with high uniaxial compressive strain in the channels. Conclusions: We have demonstrated a novel method of fabricating 3D-stacked strained SiGe/Ge GAA by 3D Ge condensation. The method allows Ge-rich SiGe and/or Ge to be incorporated in channel with a large uniaxial compressive strain. NS and NW GAA device architecture can be fabricated. Through the geometric optimization of GAA channels, the large uniaxial compressive strain of ~2.5% and the excellent electrical characteristics of the pFETs with high hole mobility of 617 cm<sup>2</sup>/Vs are demonstrated.

Reference: [1] N. Loubet et al., VLSI (2017) [2] H. Mertens et al., IEDM (2017) [3] J. Suh et al., Acknowledgement: This work was supported SSE (2016) [4] J. Suh et al., DRC (2009) [5] F. Pezzoli et al., Mat. Sci. Semicond .Proc., 11 (2008) in part by the Stanford SystemX Alliance, by the [6] S. Swaminathan et al., APL 95, 2009 [7] T.C. Pekin et al., Ultramicroscopy, 176 (2016) U.S. Naval Research Lab., by SNF and SNSF.

