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Electrical Properties of p-Channel Thin-Film Transistors Fabricated on High-Mobility Polycrystalline Ge on Glass

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Abstract

We fabricated accumulation-mode metal source/drain p-channel TFTs using high-mobility Ge formed on glass using our recently-developed solid-phase crystallization technique. The TFT using this Ge layer exhibited both high field effect mobility (170 cm^2/Vs) and on/off current ratio (~10^2) without minimizing the channel region (< 1 μm). The key technology was thinning the 100 nm thick Ge layer with a large grain size (3.7 μm) enough to fully deplete the channel.

1. Introduction

To improve the performance of Ge-thin film transistors (TFTs), it is essential not only to enhance the crystallinity of poly-Ge but also comprehensively study the relationship between its electrical properties and TFT characteristics. We recently found that the densification of amorphous Ge (a-Ge) precursor significantly enlarged the grain size of poly-Ge and improved Hall effect hole mobility μ_{Hall} of 340 cm^2/Vs in solid-phase crystallization (SPC) [1]. In the present study, we fabricate poly-Ge TFTs using SPC-Ge and discuss the relationship between the film properties (thickness, μ_{Hall}, and hole concentration p) and TFT characteristics (field-effect mobility: μ_{FE} and on/off currents). We demonstrate the highest μ_{FE} among low-temperature (< 500 °C) poly-Ge TFTs without minimizing the channel region.

2. Experimental Procedure

The a-Ge layers were deposited on SiO_2 glass substrates using the Knudsen cell of a molecular beam deposition system (base pressure: 5×10^{-7} Pa). The initial film thickness of the a-Ge layer, t_i, ranged from 25 to 200 nm. The Ge layers were densified by heating the substrate at 125 °C during deposition [1-3]. The samples were then loaded into a conventional tube furnace in an N_2 atmosphere annealed at 450 °C for 5 h to induce SPC. The grown layers were analyzed by the electron backscattering diffraction (EBSD) measurement and Hall effect measurement (van der Pauw method).

We fabricated accumulation-mode metal source/drain (S/D) p-channel TFTs using SPC-Ge. Figure 1 shows the process and structure. Pt and TiN were sequentially formed as a metal S/D and a capping layer, respectively. The PtGe/Ge contacts have low hole barrier height and are suitable for p-channel Ge-TFTs. We used Al/SiO_2/Al_2O_3/SiO_2/GeO_2 for the gate stack. The channel width and length (W/L) were 55 and 10 μm, respectively. Here, all process including SPC were conducted below 450 °C.

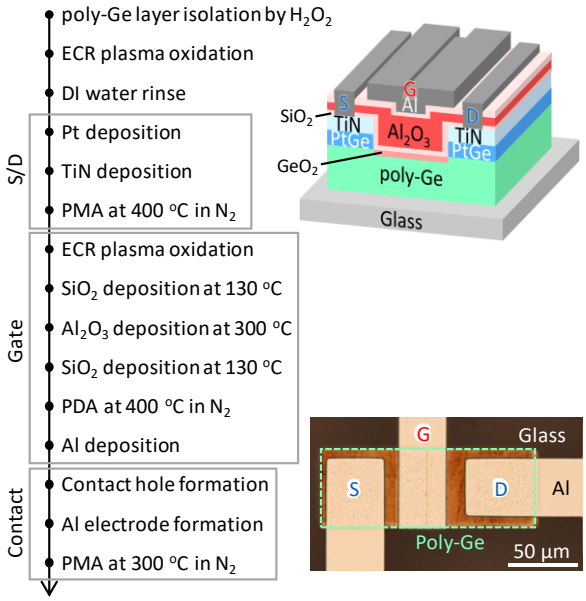

Fig. 1 Fabrication process flow (left), schematic and an optical micrograph (right) of the p-channel SPC-Ge TFTs.

3. Results and Discussion

First, we discuss the crystalline quality and electrical properties of the SPC-Ge layer. Figures 2(a)–2(e) show the grain size dramatically varies with t_i while the crystal orientation is almost random for all t_i. Figure 2(f) shows that the highest grain size is obtained at t_i = 100 nm. This behavior likely reflects the balance of the precursor density and the stress in the Ge film. All samples showed p-type conduction because the defects in Ge provides shallow acceptor levels that generate holes at room temperature. Therefore, larger grain sizes, that is, fewer grain boundaries, provide lower p, as shown in Figs. 2(f) and 2(g). Figure 2(g) also shows that μ_{Hall} peaks at t_i = 200 nm, whereas the grain size peaks at t_i = 100 nm. This behavior is likely attributed to the carrier scattering near the Ge/SiO_2 interface. Because the interface scattering is weaker for the thicker film, t_i = 200 nm exhibits the higher μ_{Hall} than t_i = 100 nm.

Finally, we discuss the TFT characteristics fabricated on SPC-Ge. Figures 3(a)–3(d) show that the drain current (I_D)-gate voltage (V_G) and μ_{FE} characteristics vary significantly with t_i. Figure 3(e) shows on-current I_{on}, off-current I_{off}, and on/off current ratio I_{on}/I_{off} estimated from the I_D-V_G characteristics. I_{on} increases with increasing t_i, which reflects μ_{Hall} (Fig. 2(g)) and exhibits high values (> 10^{-4} A) at $t_i \geq 100$ nm. I_{off} is determined by the relationship between t_i and the maximum

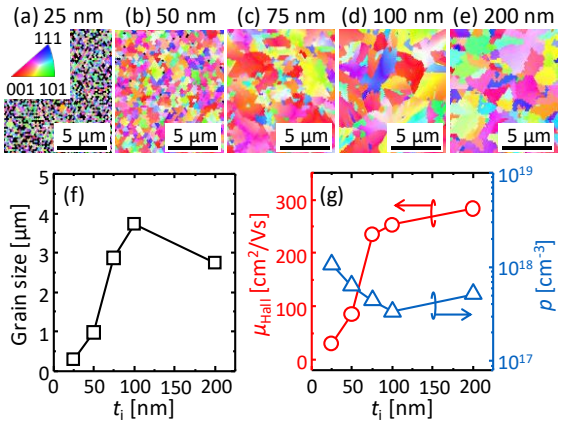

Fig. 2 Initial film thickness t_i dependence of the grain size and electrical properties of the SPC-Ge layers.

depletion layer width d_{max}, which can be estimated from p. For example, the d_{max} of Ge when $p = 3 \times 10^{17}$ cm^{-3} is approximately 54 nm, assuming that the dielectric constant and intrinsic carrier concentration of Ge are 16 and 2.4×10^{13} cm^{-3} at room temperature, respectively. From the relationship between d_{max} and t_i, we found that the lower t_i provides the higher occupation of the depletion layer in the whole SPC-Ge layer, which decreases I_{off} (Fig. 3(e)). Reflecting I_{on} and I_{off}, the I_{on}/I_{off} reaches the maximum at t_i = 50 nm. Figure 3(f) shows that μ_{FE} is consistent with the trend of μ_{Hall} reflecting the properties of SPC-Ge, while μ_{FE} is much lower than μ_{Hall}. This is likely because not only carrier scattering at the MOS interface, but also large I_{off} causes underestimation of g_m and μ_{FE}. To overcome this problem, a Ge layer compatible with high μ_{Hall} (corresponding high I_{on}) and a thin film (corresponding low I_{off}) is desirable.

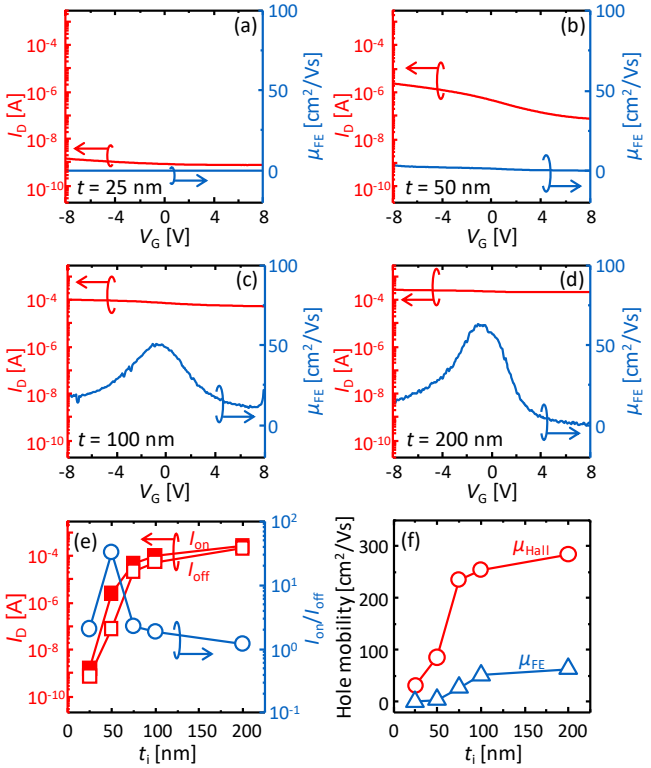

Fig. 3 Electrical properties of p-channel SPC-Ge TFTs with various initial film thickness t_i, where $V_D = -0.1$ V.

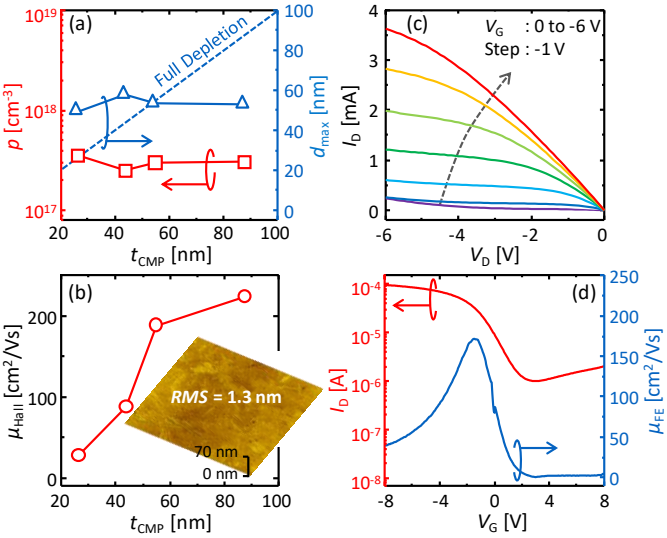

Fig. 4 (a),(b) In-depth profiles of electrical properties for SPC-Ge layers for initial film thickness t_i = 100 nm. Inset in (b) shows atomic force micrograph of SPC-Ge thinned to t_{CMP} = 55 nm with scan region of 10 × 10 μm^2. (c) I_D-V_D characteristics and (d) I_D-V_G characteristics and field-effect mobility μ_{FE} at V_D = −0.1 V for the SPC-Ge TFT thinned to t_{CMP} = 55 nm.

We thinned the t_i = 100 nm sample, which has the largest grain size (Fig. 2(f)), using chemical-mechanical polishing (CMP). Figure 4(a) shows that p is constant in the depth direction. According to d_{max} estimated from p, full depletion in SPC-Ge is obtained when the thinned film thickness t_{CMP} is below 55 nm. Conversely, μ_{Hall} decreases significantly for t_{CMP} < 50 nm (Fig. 4(b)), likely reflecting carrier scattering at the Ge/SiO$_2$ interface. Therefore, we determined that t_{CMP} = 55 nm is almost optimal for achieving both high μ_{FE} and I_{on}/I_{off}. The t_{CMP} = 55 nm sample showed a smooth surface (Fig. 4(b), root mean square value: 1.3 nm) and the same grain size as before CMP. This sample was processed into TFTs by the procedure shown in Fig. 1. Figure 4(c) shows the typical p-channel transistor operation, i.e., the I_D increases with increasing V_G. Figure 4(d) shows high I_{on}/I_{off} (10^2) and μ_{FE} (170 cm^2/Vs) because of both the high I_{on} due to the high μ_{Hall} and low I_{off} due to the thin thickness (55 nm) in SPC-Ge. The current TFT performance is the highest among simple poly-Ge TFTs formed on glass and will be further improved by nanofabrication processes such as miniaturization of the channel region and multi-gate structure.

4. Conclusion

We comprehensively studied the relationship between poly-Ge thin film properties and accumulation-mode TFT characteristics. By thinning the 100 nm thick Ge layer with a large grain size (3.7 μm) enough to fully deplete the channel, we demonstrated high performance TFT with both high field effect mobility μ_{FE} (170 cm^2/Vs) and on/off current ratio (~10^2). This is the highest μ_{FE} among low-temperature (< 500 °C) polycrystalline Ge TFTs without minimizing the channel region (< 1 μm).

References

[1] K. Toko, K. Moto *et al.*, Sci. Rep. **7**, 16981 (2017).
[2] K. Moto *et al.*, Sci. Rep. **8**, 14832 (2018).
[3] K. Moto *et al.*, Appl. Phys. Lett. **114**, 112110 (2019).