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Experimental demonstration of n- and p-channel GaN MOSFETs operation for power IC

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Abstract

N- and p-channel GaN MOSFETs with a Ni/Al_2O_3 gate stack structure are fabricated and evaluated. For the first time, n- and p-channel MOSFETs' operations are successfully demonstrated. Additionally, it is found that the high-temperature post-deposition annealing at around 700°C is effective for the MOSFETs operation.

1. Introduction

A GaN power integrated circuit (IC) consisting of GaN logic circuits is a promising candidate for a future power IC with a low power consumption and high performances. In order to realize the GaN power IC, n- and p-channel MOSFETs with high performances are mandatory. Recently, a very low interface trap density (D_{it}) near the conduction band edge (CBE) has been reported in n-GaN [1]. On the other hand, in the case of p-GaN, poor MOS properties have been reported [2], suggesting that D_{it} near the valence band edge (VBE) could be much higher than that near CBE. The large number of the interface traps could induce Fermi level pinning (FLP), which might be one of the origins for the difficulty of p-channel GaN MOSFET operation. In this study, in order to demonstrate n- and p-channel GaN MOSFETs' operations with the same gate stack structure, the inversion mode n-channel and accumulation mode p-channel GaN MOSFETs are fabricated and evaluated.

2. Experimental procedure

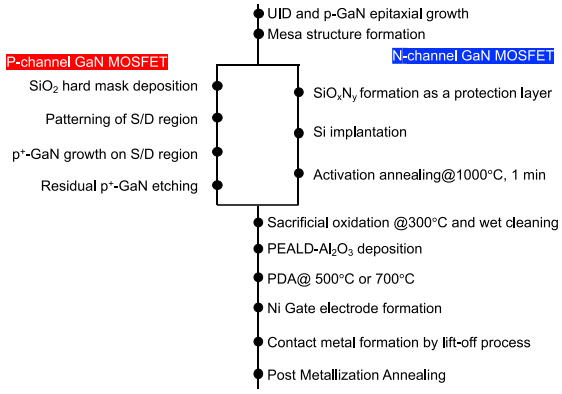

Fig. 1 : Fabrication process flows for the GaN MOSFETs

The fabrication process is shown in Fig. 1. A 500-nm-thick p-GaN (Mg: 2×10^{17}cm^{-3}) layer is grown by metal organic chemical vapor deposition on a semi-insulating GaN substrate with a thin unintentionally doped GaN (UID-GaN). Mesa structures using the p-GaN layer are formed using the conventional lithography technique, wet and dry etchings. For the n-channel MOSFET, Si atoms are implanted into the source and drain (S/D) regions separated by a photoresist dummy gate and a 10-nm-thickness SiO_xN_y protection layer. The dopant atoms are activated by the rapid thermal annealing in a N_2 atmosphere. In the p-channel MOSFET, the p^+-GaN layer (Mg: ~10^{20} cm^{-3}) is grown on the S/D regions separated by the SiO_2 hard mask layer to reduce contact resistance between contact

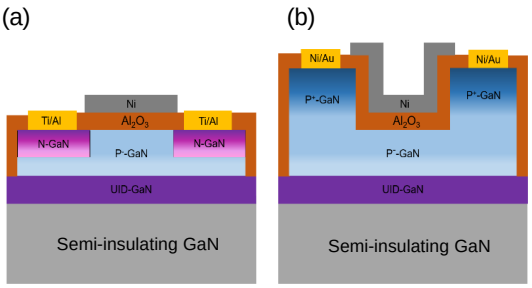

Fig. 2 : Schematic cross-sectional views of (a) n- and (b) p- channel GaN MOSFETs

metals and the p-GaN layer. Subsequently, the sacrificial ozone oxidation of the p-GaN layer is performed to reduce the process damage in the channels. Subsequently, the 30-nm-thick Al_2O_3 layer is formed on the p-GaN layers using the enhanced plasma atomic layer deposition (PEALD). In order to modulate interface properties, post deposition annealing (PDA) is performed in a N_2 ambient condition. Ni gate electrodes are formed using the thermal evaporation method. The Ti/Al and Ni/Au contact metals are formed on the S/D regions of n-type and p-type GaN layers, respectively. Finally, post-metallization annealing is performed to obtain the ohmic contacts. The cross-sectional views of the fabricated MOSFETs are shown in Figs. 2(a) and 2(b).

3. Results and discussion

Band-bending behavior in the GaN surface strongly depends on MOS interface properties. The relationship between the gate-to-channel capacitance (C_{gc}) and gate voltage (V_g) gives us some information related to the MOS interface properties. Figure 3 shows the C_{gc}-V_g curves of the n-channel MOSFETs. In the negative V_g bias, the C_{gc} values are almost zero without depending on the PDA temperature. Subsequently, the C_{gc} values increase around V_g = 1V. Moreover, in the V_g ranging from 1.5 to 6 V, clear accumulation behaviors are observed for all n-channel

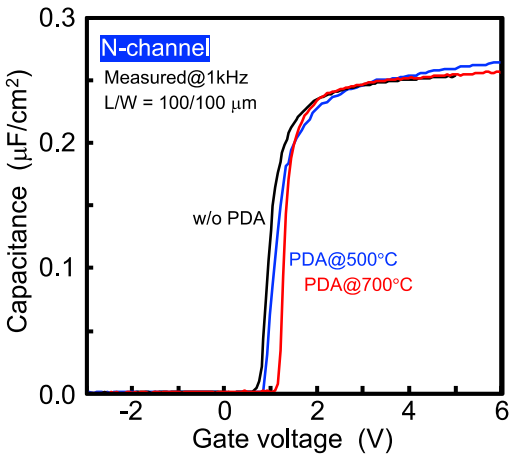

Fig. 3: C_{gc}-V_g curves of the n-channel MOSFETs for the various PDA conditions.

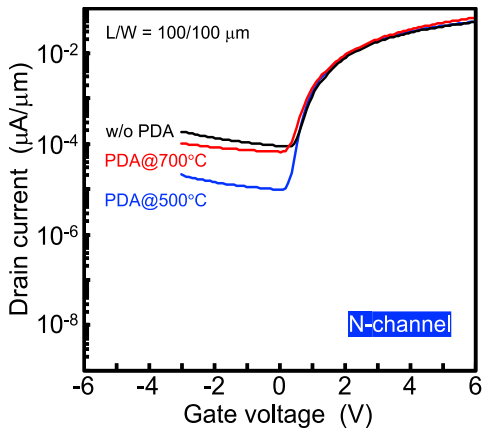

Fig. 4: I_d-V_g curves of the n-channel MOSFETs for the various PDA conditions.

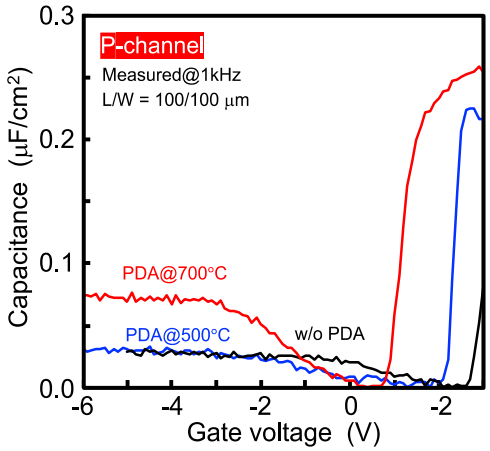

Fig. 5: C_{gc}-V_g curves of the p-channel MOSFETs for the various PDA conditions.

MOSFETs. These results suggest that the band-bending conditions can be controlled by the gate voltage. The good gate controllability results in clear cut-off properties of drain current (I_d)-V_g characteristics (Fig. 4). It should be noted that I_d of the device treated by the PDA at 700°C is higher than those of devices treated by the PDA at 500°C and without the PDA. This might be owing to the improvement of the MOS interface properties by PDA at 700°C.

In contrast, the p-channel MOSFETs indicate different C_{gc}-V_g curves from the n-channel MOSFETs (Fig. 5). In the V_g ranging from 0 to -6 V, the C_{gc} values are much smaller than those of the accumulation bias condition, as shown in Fig. 3. This might be attributable to the insufficient gate controllability due to FLP. In spite of the insufficient gate controllability, the C_{gc} value of the device annealed at 700°C is higher than those of the other conditions, suggesting that the PDA at 700°C can improve the MOS interface properties near VBE. Indeed, I_d-V_g characteristics of devices whose Al_2O_3 dielectrics are treated by the PDA at 500°C and without PDA do not show cut-off properties (Fig. 6). In contrast, the device annealed at 700°C indicates a good cut-off property in I_d-V_g curve (Fig. 6). However, the drain on-current is much lower than those of the n-channel MOSFETs. Also, in Fig. 5, the C_{gc} values are observed in the positive V_g bias. The reason of the observation of the C_{gc} in the accumulation mode p-channel MOSFETs is still unclear. Further study and improvement of the MOS interface properties near VBE are mandatory.

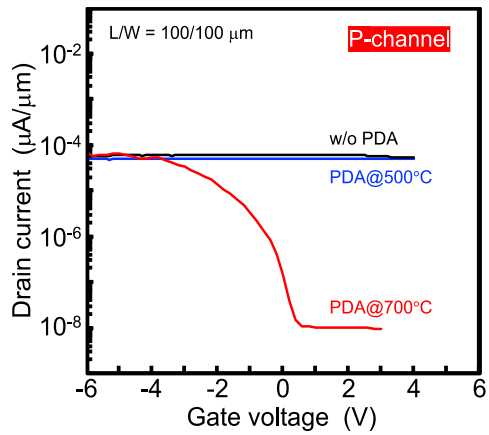

Fig. 6: I_d-V_g curves of the p-channel MOSFETs for the various PDA conditions.

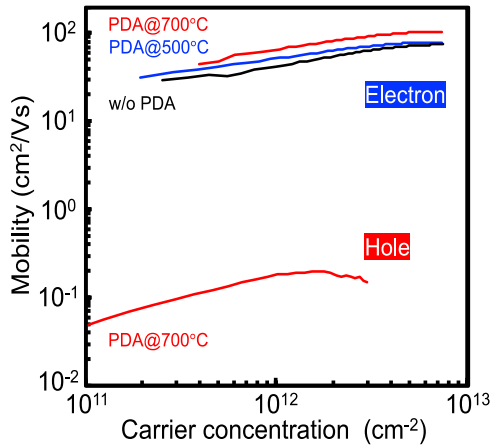

Fig. 7: Electron and hole mobilities as a function of the carrier concentration.

Electron and hole mobilities are extracted from the I_d-V_g and C_{gc}-V_g characteristics. The mobilities as a function of the carrier concentration are shown in Fig. 7. Electron mobilities are around 30 to 100 cm^2/Vs. Maximum hole mobility is 0.2 cm^2/Vs. For the both channel, PDA at 700°C results in the highest mobility, suggesting that high temperature PDA is effective for improving the MOS interface properties. On the other hand, the both electron and hole mobilities decrease with the increase of the carrier concentration in the wide range of the carrier concentration. This indicates the existence of a large number of Coulomb scattering centers. We find that there is a possibility that higher electron and hole mobilities can be achieved by further improvement of the MOS interface properties.

4. Conclusions

The n- and p-channel GaN MOSFETs with the Ni/Al_2O_3 gate stack structure are fabricated under various PDA conditions. Although, in the case for without PDA and PDA at 500°C, the p-channel MOSFETs did not show the cut-off properties, PDA at 700°C leads the good cut-off properties for the both channel MOSFETs and high electron and hole mobilities.

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References:

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