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Implementation of FeFET Memory Device Utilizing Highly Reliable Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Film with Embedded Al Nanoclusters

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Abstract

This paper demonstrates ferroelectric field effect transistors (FeFETs) utilizing ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) films with embedded Al nanoclusters. The data retention capability for 10 years at 150 °C was ensured even for sub-micron scaled FeFETs. This highly reliable FeFET is a promising candidate for future non-volatile memory application.

1. Introduction

Ferroelectric field effect transistors (FeFETs) based on doped hafnium oxide (HfO_2) thin films attract more attention as future embedded nonvolatile memories because of scalability and CMOS compatibility [1]. In particular, Zr doped HfO_2 films (HZO) show ferroelectricity with high remnant polarization (P_r) [2,3]. However, there are few reports on reliability of HZO-based FeFET memories in sub-micron scale. Recently, it has been reported that embedding Al nanoclusters in HZO film improves reliability of the metal-ferroelectric-metal (MFM) capacitor, as shown in Fig. 1 [4]. In this study, we fabricated sub-micron scaled FeFET with metal-ferroelectric-insulator-silicon (MFIS) structure utilizing the ferroelectric HZO film with embedded Al nanoclusters and demonstrated their memory characteristics.

2. Experimental

Fig. 2 shows the fabrication flow of FeFETs based on HZO films with embedded Al nanoclusters. This process is the same as conventional CMOS process except for a gate stack. 1-nm-thick SiO_2 interlayer (IL) was formed on a p-type well by thermal oxidation. Then, 10-nm-thick HZO film (Hf:Zr = 1:1) was deposited on IL by atomic layer deposition at 300 ºC. Al at the dose of 5×10^{13} cm^{-2} was embedded in the middle of HZO films [4]. After depositing 10-nm-thick TiN capping layer by sputtering, rapid thermal annealing at 600 ºC was carried out to form the ferroelectric phase of HZO film. After 100-nm-thick poly-crystalline Si was stacked by low-pressure chemical vapor deposition, gate patterning and the spacer formation were carried out. To form source and drain, activation annealing was performed after As and P implantation. Finally, contact and metallization were formed.

Memory characteristics were evaluated on FeFETs with the various gate length (L_g: 120 ~ 3200 nm) and gate width (W_g: 300 ~ 5200 nm). The gate voltage for program and erase (P/E) operation of FeFETs were -5 and 5 V, respectively. These amplitudes were adequate for saturation of V_{th} changes in P/E operation. While retention characteristics was evaluated at 150 ºC, P/E operation and the V_{th} read were conducted at room temperature.

3. Results and Discussion

Fig. 3 shows forward and reverse I_d-V_g curves of the FeFET. The counterclockwise hysteresis loop shows the ferroelectric behavior. Fig. 4 indicates program and erase characteristics of the FeFET. The P/E speeds are about 1 and 10 μs, respectively. Fig. 5 shows the dependence of memory windows (MWs) on the gate area (= $L_g \times W_g$). The MWs get narrower in small gate area below 0.3 μm^2. The phenomena that MWs get narrower for smaller FeFETs are accounted for by charge trapping during P/E operation [5]. Fig. 6 show endurance characteristics of short and long channel FeFETs. After 10^3 P/E cycles, the MW of the short channel FeFET gets narrower approximately 20 % compared to that of the long channel FeFET. Fig. 7 shows TEM cross section of the FeFET. A pitting of HZO films was observed at the gate edge, which indicates that the HZO films was damaged during gate etching. The gate edge pitting might cause the degradation of polarization switching for the short channel FeFET. To avoid pittng at the gate edge, further process optimizations are needed. On the other hand, in retention characteristics, decay rate of short channel FeFET is comparable to that of long channel, as shown in Fig. 8. These results imply that the impact of gate edge component on polarization retention is smaller than that on polarization switching. Furthermore, even though the channel length is 120 nm, the MW degradation is estimated less than 50 % after 10 years at 150 ºC. This result has shown for the first time that the HZO-based FeFET memory in sub-micron scale has high reliability.

3. Conclusions

Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) film with embedded Al nanoclusters was successfully implemented on FeFETs. Data retention capability for 10 years was ensured at 150ºC for FeFETs scaled to sub-micron orders for the first time. FeFETs with highly reliable HZO films with embedded Al nanoclusters are suitable for future reliable memory devices.

References

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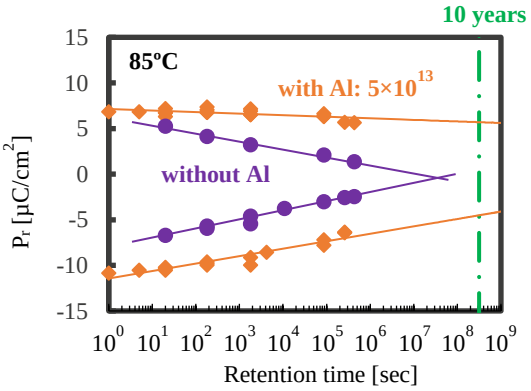

Fig. 1 Retention characteristics of MFM capacitor with/without Al-nanoclusters in HZO film at 85°C [4].

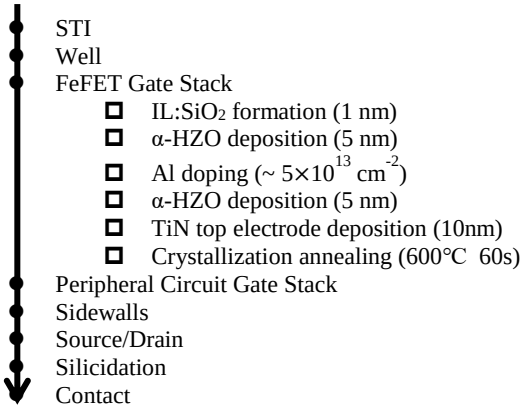

Fig. 2 Process flow of HZO FeFET

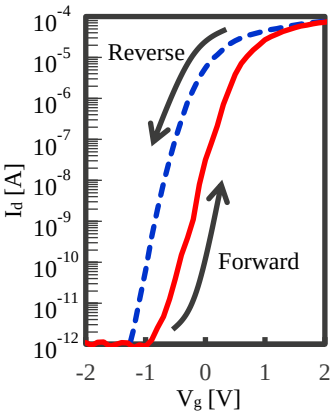

Fig. 3 I_d-V_g characteristics in both forward and reverse sweep directions in FeFET.

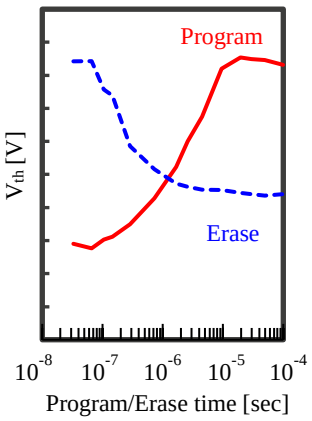

Fig. 4 Program/Erase characteristics of FeFET (L_g/W_g = 200/300 nm).

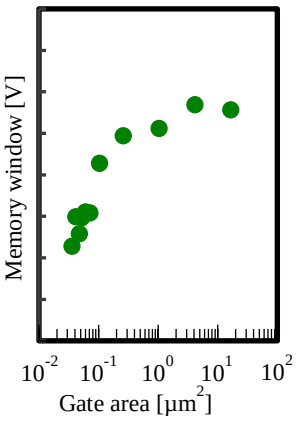

Fig. 5 Dependence of MW in FeFETs on the gate area.

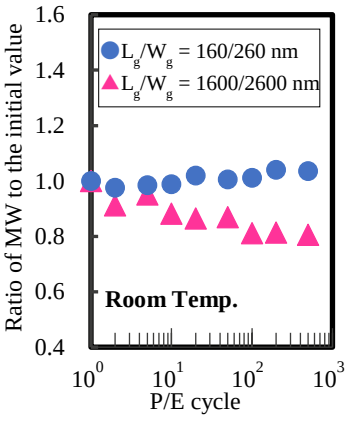

Fig. 6 Endurance characteristics of MW in FeFETs with program (V_g = -5 V, 10 μs) and erase (V_g = 5 V, 10 μs) bipolar cycle.

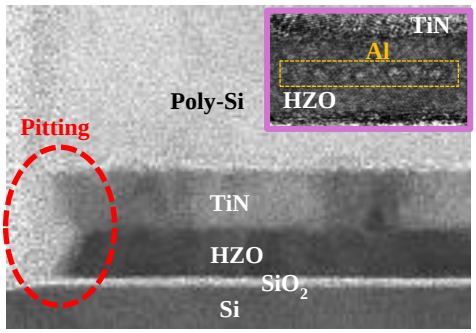

Fig. 7 Cross sectional TEM image of HZO-based FeFET. The inset shows Al nanoclusters embedded in the HZO film.

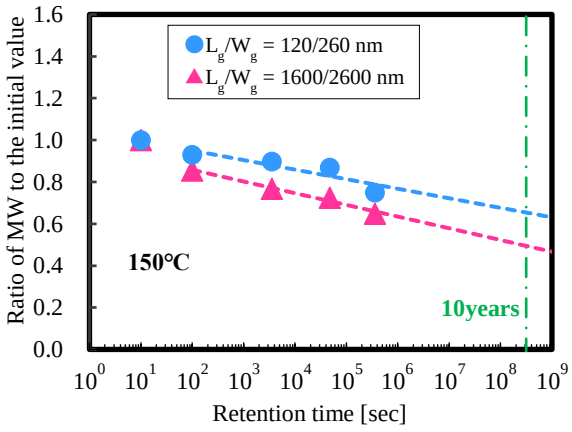

Fig. 8 Retention characteristics of MW in FeFETs with long and short channels, respectively.