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Performance improvement in ZnSnO/Si bilayer TFET by W/Al_2O_3 gate stack

K. Kato[1,2], H. Matsui[2], H. Tabata[2], T. Mori[1], Y. Morita[1], T. Matsukawa[1], M. Takenaka[2], and S. Takagi[2]

[1]National Institute of Advanced Industrial Science and Technology, 1-1-1, Umezono, Tsukuba, Ibaraki 305-8568, Japan

[2]The University of Tokyo, 7-3-1 Hongo, Bunkyo, Tokyo, 113-0032, Japan

TEL: +81-29-849-1531, FAX: +81-29-861-5170, E-mail: kimihiko.kato@aist.go.jp

Abstract - We have examined impact of gate insulator (Al_2O_3 or HfO_2) and gate electrode (TiN or W) on performance of ZnSnO/Si bilayer TFETs. It is found that the W/Al_2O_3 gate stack is suitable for the ZnSnO channel TFETs. By combined with PMA at appropriate temperature, the hysteresis-free steep on/off switching with minimum *S.S.* of 65.4 mV/dec. has been realized in W/Al_2O_3/ZnSnO/Si bilayer n-TFETs.

1. Introduction

In order to increase on-state current (I_{on}) of tunneling field effect transistors (TFETs) without increasing the off-state leakage current, a hetero tunneling junction with type-II energy band alignment is the most promising [1-3]. Additionally, a bilayer structure is another attractive approach to increase I_{on} [4]. Recently, we have proposed a bilayer TFET structure composed of the hetero-tunneling junction of an n-type oxide semiconductor (n-OS) and a p-type group-IV semiconductor (p-IV), which can realize the above two approaches at the same time [5]. TCAD simulation has predicted that the extremely-small sub-threshold swing (*S.S.*) of as small as ~1 mV/dec. can be expected in the proposed n-OS/p-IV bilayer TFET.

However, the experimentally-achieved *S.S.* values of the Zn(Sn)O/(Si,Ge) bilayer TFETs so far are higher than 71 mV/dec., which have a large gap with the simulated results [5,6], suggesting the necessity of further improvement of the metal/high-*k*/OS gate stack structures. The quality of the gate stacks could be sensitive to materials of the gate metal/insulator and the process condition because the oxygen concentration drastically changes the characteristics of OS [7]. In this study, therefore, we have examined the impact of the gate electrode, the gate insulator and PMA temperature on the electrical performance of TFETs.

2. Device fabrication process

The n-ZnSnO/p-Si bilayer TFETs were fabricated on a p^+-Si(100) source ($N_a = 4\times10^{19}$ cm^{-3}) as shown in Fig. 1. First, an SiO_2 passivation layer and an ITO buried drain were formed, and a window for the tunneling junction was chemically formed by BHF. Then, the amorphous ZnSnO channel layer with a Zn/Sn ratio of 1.5 was deposited by PLD at 300°C to realize high thickness uniformity [6]. Subsequently, the gate stack was formed as follows. 1 nm-thick ALD-Al_2O_3 was deposited and plasma oxidation was performed to reduce the interface state density. Then, 9 nm-thick Al_2O_3 or 7 nm-thick HfO_2 layer was successively deposited, followed by annealing at 350°C in O_2 ambient. After this, the W gate electrode was formed. The TiN gate was also used in comparison. Consequently, three types of the gate stacks, TiN/Al_2O_3, W/Al_2O_3 and W/HfO_2/Al_2O_3, were prepared and compared. Finally, Ni source was formed and PMA was carried out. Here, PMA temperature (T_{PMA}) was varied to study the impact on the device characteristics.

3. Results and discussion

First, we evaluated the gate stack quality from the *C-V* characteristics (Fig. 2), where the source and the drain were grounded and the gate bias voltage was varied. Fig. 3 summarizes the capacitance equivalent thickness (CET) and the hysteresis voltage width (V_{hys}) of each sample. The CET values of the TiN/Al_2O_3, W/Al_2O_3, and W/HfO_2/Al_2O_3 gate stacks are 5.5, 5.9, and 2.3 nm, respectively. In the conventional TiN/Al_2O_3 gate stack, a large counter clockwise hysteresis is observed, indicating the existence of any mobile ions. In contrast, V_{hys} is drastically reduced by using the W gate for both Al_2O_3 and HfO_2/Al_2O_3 samples, indicating the superiority of the W gate.

The electrical characteristics of these TFETs with the W gate electrode were compared by changing T_{PMA} (Fig. 4). The characteristics of the W/Al_2O_3 TFET are very sensitive to T_{PMA}. It is found that T_{PMA} of 350-360 °C can provide the best performance with the high I_{on}/I_{off} ratio and the low *S.S.* (Fig. 5). Lower T_{PMA} suppresses I_{on}, while higher one degrades *S.S.* and the cut-off properties significantly. In contrast, the characteristics of the W/HfO_2/Al_2O_3 TFETs have less T_{PMA} dependence up to 300°C.

The sub-threshold characteristics of these two TFETs with optimal T_{PMA} are studied in detail. With the W/Al_2O_3 gate stack, the minimum *S.S.* value of 65.4 mV/dec. has been realized in this TFET, which is the lowest value obtained in n-OS/p-IV bilayer TFETs so far (Fig. 6(a)). Here, there is almost no difference between *S.S.* values estimated from I_d and I_s over the wide current range, because I_g of the W/Al_2O_3 gate stack is sufficiently low. Additionally, it is also found that the present W/Al_2O_3 TFET can realize both almost hysteresis-free sub-threshold characteristics and well-behaved output characteristics (Figs. 7 and 8). On the other hand, the minimum *S.S.* value of the W/HfO_2/Al_2O_3 TFET is higher than 70 mV/dec. (Fig. 6(b)), although CET of this TFET is roughly 1/3 of CET of the W/Al_2O_3 TFET. Also, *S.S.* estimated from I_d increases in the low I_d region (< 10^{-6} μA/μm) in comparison with *S.S.* estimated from I_s, because I_g contaminates I_d in the low I_d region.

Finally, the impacts of the present gate metals and gate insulators are summarized. The W gate is effective for improvement of not only minimum *S.S.* but also average *S.S.*, estimated over the V_g swing of 0.3 V (Fig. 9). The relationship between CET and *S.S.* is shown in Fig. 10. It is found the improvement of the OS interfacial quality is more essential for the improvement of the sub-threshold characteristics than EOT scaling. In addition, the present results show that the interface properties and resulting *S.S.* in TFETs are strongly modulated by the choice of high-*k* and gate metal materials even for the same Al_2O_3/ZnSnO interfaces. These dependencies could be attributed to the difference in oxygen migration among the different gate stacks, because the high-k/ZnSnO interfaces can be sensitive to oxygen or oxygen vacancies. For example, the W gate might reduce the magnitude of oxygen subtraction (*ie.* scavenging effect), whereas ALD-HfO_2 might contain larger amount of excess oxygen than Al_2O_3. As a result, we can interpret that the W/Al_2O_3 gate stack can minimize oxygen migration and the related chemical reactions at the interface, leading to the reduction in the defect density at the Al_2O_3/ZnSnO interface and the resulting lower *S.S.*

5. Conclusions

We examined the impact of the gate insulator and the gate electrode on the sub-threshold characteristics of the ZnSnO/ Si bilayer TFETs. The W/Al_2O_3 gate stack with PMA at 350 ºC has been found to realize the hysteresis-free I_d-V_g characteristic with the minimum *S.S.* value of 65.4 mV/dec. The present result has revealed that the improvement of the gate stack quality is more effective in realizing both low *S.S.* and low I_{off} than the EOT scaling.

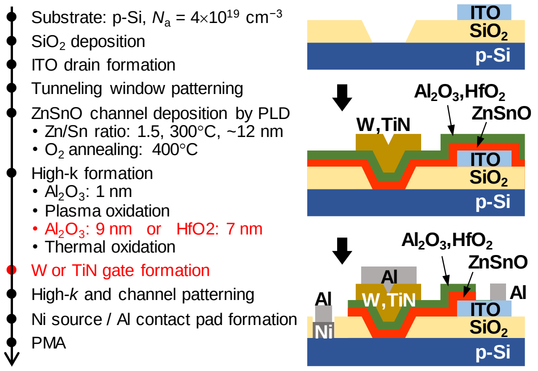

Fig. 1 n-ZnSnO/p-Si bilayer TFET fabrication flow. Impacts of Al_2O_3 or HfO_2 gate insulator and W or TiN gate electrode were examined.

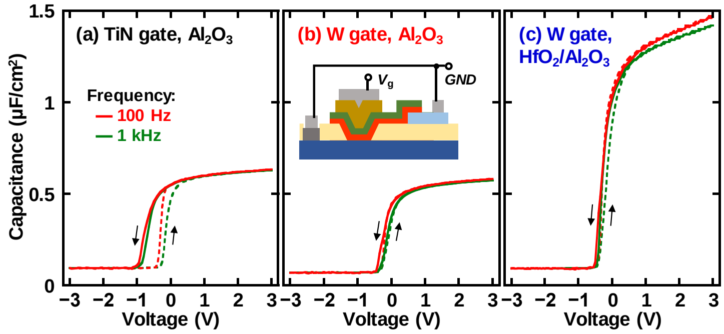

Fig. 2 C-V characteristics of metal/high-k/ZnSnO MOS capacitors with (a) TiN/Al_2O_3, (b) W/Al_2O_3 and (c) W/HfO_2/Al_2O_3.

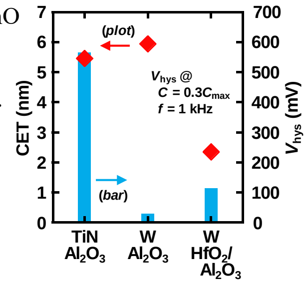

Fig. 3 CET and V_{hys} of each gate stacks.

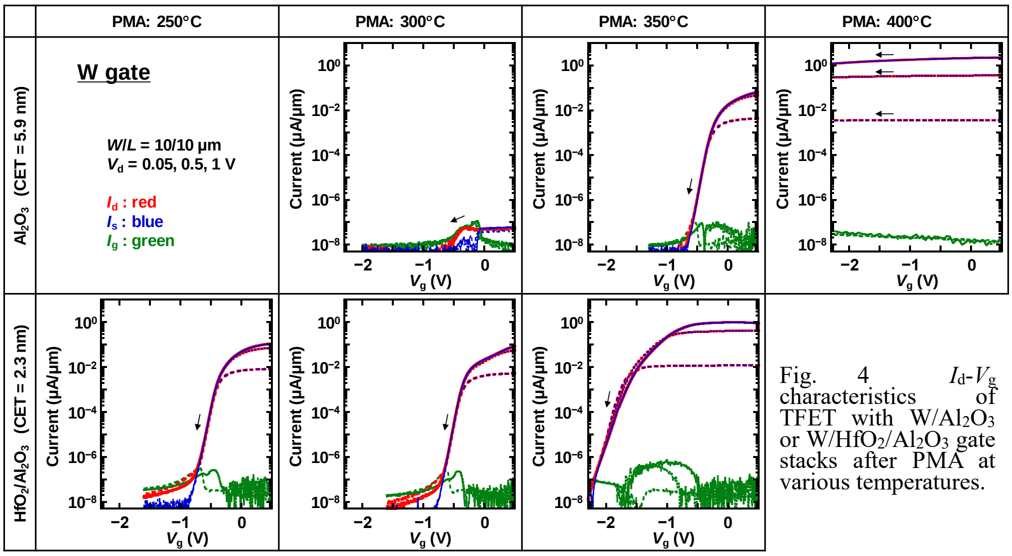

Fig. 4 I_d-V_g characteristics of TFET with W/Al_2O_3 or W/HfO_2/Al_2O_3 gate stacks after PMA at various temperatures.

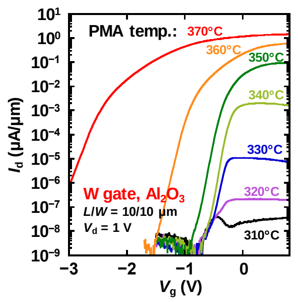

Fig. 5 Impact of PMA temperature on I_d-V_g characteristics of TFET with W/Al_2O_3 gate stack.

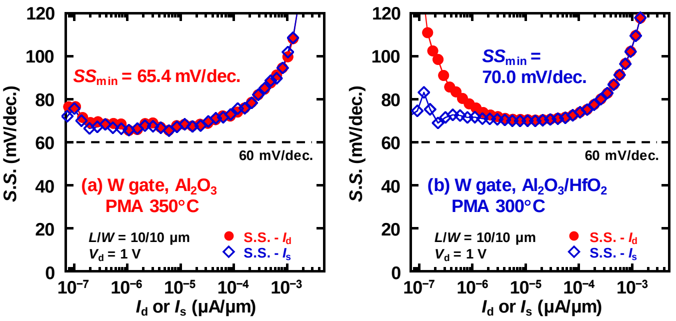

Fig. 6 $S.S.$-I_d and $S.S.$-I_s characteristics of TFET with (a) W/Al_2O_3 and (b) W/HfO_2/Al_2O_3 gate stacks.

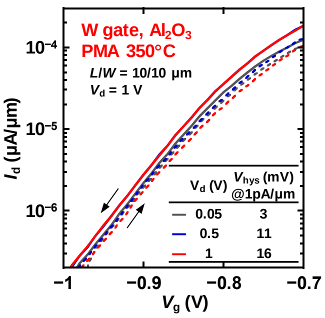

Fig. 7 Double sweep I_d-V_g of W/Al_2O_3 TFET in sub-threshold region.

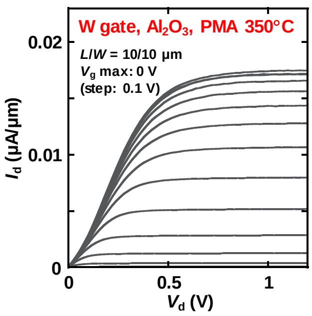

Fig. 8 I_d-V_d characteristics of W/Al_2O_3 TFET.

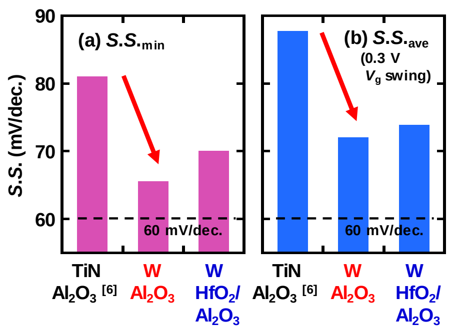

Fig. 9 Impact of gate stacks on (a) minimum $S.S.$ and (b) average $S.S.$ in 0.3 V-V_g swing.

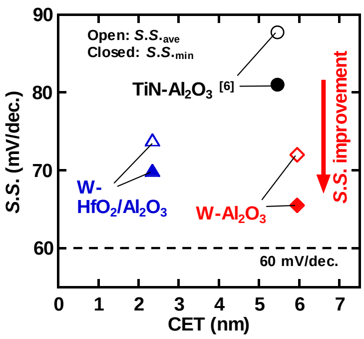

Fig. 10 Relationship between CET and $S.S.$ of ZnSnO/Si bilayer TFET with various gate stacks.

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References: [1] X. Zhao *et al*. Tech. Dig. IEDM 2014, p.590. [2] M. Kim *et al*., Tech. Dig. IEDM 2014, p.331. [3] T. Gotow *et al*., J. Appl. Phys. **122**, 174503 (2017). [4] L. Lattanzio *et al*., IEEE Elec. Dev. Lett. **33**, 167 (2012). [5] K. Kato *et al*., Tech. Dig. IEDM 2017, p.377. [6] K. Kato *et al*., Tech. Dig. EDTM 2019, SiDev2-1. [7] K. Kato *et al*., Appl. Phys. Lett. **112**, 162105 (2018).