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Demonstration of n- and p-TFET operations in a single ZnSnO/SiGe bilayer structure

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Abstract

We have proposed p-TFET operation in a bilayer TFET composed of an n-type oxide-semiconductor and p-type group-IV semiconductor. TCAD simulation has predicted a symmetric n-/p- operations. Moreover, we have experimentally demonstrated the p-TFET operation by using a ZnSnO/SiGe-OI TFET under Si back gate operation. Both n- and p-TFET operations are also observed in an identical device by changing the gate electrodes between the top and back ones.

1. Introduction

A bilayer tunneling field effect transistor (TFET) is one of attractive device structures to realize high on-state current (I_{on}) and low sub-threshold swing (*S.S.*) thanks to vertical band-to-band tunneling (BTBT) over the entire region of the tunneling junction [1]. Recently, we have proposed a bilayer TFET composed of the hetero-tunneling junction of an n-type oxide semiconductor (n-OS) and a p-type group-IV semiconductor (p-IV) with type-II energy band alignment and have experimentally demonstrated the operation [2]. We have also presented the improvement of the sub-threshold characteristics by using an amorphous ZnSnO channel [3,4].

One of remaining challenges to apply the n-OS/p-IV bilayer TFETs into real circuits is to realize p-type TFET operation for complementary TFET circuits. In this study, therefore, we present key ideas to realize p-TFETs and demonstrate the p-TFET operation by combination of the present bilayer TFET structure with the SiGe-on-insulator (SiGeOI) technology [5,6]

2. Concept of complementary bilayer TFET

An essence to determine the TFET operation type, n-type or p-type, is the order of staking the two layers, n-OS and p-IV, beneath the gate stack (Fig. 1). For n-TFETs already proposed, positive gate bias (V_g) bends the surface potential of the n-OS channel and electrons in the p-IV source can tunnel into the n-OS channel. Symmetrically, for p-TFETs, negative V_g bends the surface potential of the p-IV channel and electrons in the p-IV channel can tunnel into the n-OS source. Here, the remaining holes flow toward the drain, resulting in the p-TFET operation. The complementary TFETs can be realized not only the planar way but also 3D stack structures as shown in Fig. 2. The 3D stacked same n-OS/p-IV TFET structures with front and back gates allow us to realize the complementary TFET with compact layout. Actually, TCAD simulation shows that a hetero-junction composed of same materials of n-ZnO and p-Ge with both thicknesses of 10 nm can realize n- and p-TFET operations simultaneously (Figs. 3-5). It is found here that the symmetrical operation of n- and p-TFETs is realized by an appropriate choice of work function of the gate metal (Fig. 5). These results indicate that complementary TFET operation can be realized by using a single n-OS/p-IV bilayer structure with an appropriate thickness and work function of the gate metal.

3. Device fabrication

In order to demonstrate the proposed p-TFET operation, bilayer TFETs composed of p-type SiGeOI and n-type ZnSnO layers were fabricated (Fig. 6). The SiGe layer with the thickness of 15 nm and the Ge fraction of 59% (Fig. 7) was fabricated by the Ge condensation technique [5,6]. The BOX thickness was 25 nm. The ZnSnO layer with the Zn/Sn ratio of 1.5 and the thickness of 12 nm was deposited by PLD. Then, a W/Al_2O_3 top gate stack was formed. The appropriate plasma and thermal treatments were performed to improve the interface quality [7]. Ni and ITO contact electrodes were formed on SiGe and ITO layers, respectively. Fig. 8 shows the cross sectional TEM images around the ZnSnO/SiGe tunneling junction. The stacked layers of amorphous ZnSnO and single-crystal SiGe are observed (Fig. 8(b)). On the other hand, the interfacial layer between ZnSnO and SiGe layers looks thicker (~3 nm) than that of the ZnSnO/Si junction (~1.5 nm) [4], attributable to easier oxidation of Ge. We have confirmed the steep on/off switching with almost no hysteresis in a reference ZnSnO/Si TFET fabricated on a bulk Si source (Fig. 9).

4. Demonstration of n- and p-type bilayer TFETs

Both n- and p-TFET operations in a single ZnSnO/SiGe bilayer TFET were experimentally examined by selecting the appropriate gate electrodes, top or back one. Fig. 10 shows the measurement configurations of the terminals of TFETs. For p-TFET operation, under the conditions of negative bias to the p-SiGe drain and ground to n-ZnSnO source, the Si substrate is used as the gate electrode with the W top gate floating. For n-TFET operation, on the other hand, under the conditions of positive bias to the n-ZnSnO drain and ground to the p-SiGe source, the W electrode is used as the gate electrode with the Si back-gate floating.

The electrical characteristics of n- and p-TFETs are shown in Figs. 11 and 12. It is found that the clear on/off switching is obtained in the p-TFET controlled by the back gate (Fig. 11(a)). This is the first experimental demonstration of the p-TFET operation of bilayer TFETs. On the other hand, *S.S.* is as high as 900 mV/dec. This high *S.S.* value could not be simply explained by the thick back gate insulator. Improvement of the interfacial quality at the SiGe/BOX interface is expected to provide lower *S.S.* We have also confirmed the n-TFET operation in the same device (Fig. 11(b)). The steep on/off switching, which is comparable to in the reference ZnSnO/Si TFET, is realized even in the TFET with the SiGeOI source. The minimum *S.S.* value is slightly higher (~ 91 mV/dec.).

Furthermore, the achieved I_{on} value of the p-TFET is in the similar level to that of n-TFET, as expected TCAD simulation. This symmetric I_{on} is attractive for the complementary TFET circuits. On the other hand, the higher off-current of p-TFET, which is probably due to the ambipolar band-to-band tunneling in the SiGe layer under the large positive V_g, needs to be suppressed for low-power application with low off-state leakage currents.

5. Conclusions

In this study, we have presented the key idea to realize p-TFET operation in n-OS/p-IV bilayer TFETs and have found through TCAD simulation that a symmetric n-/p- operations can be expected under the same TFET structure. Furthermore, we have experimentally demonstrated the p-TFET operation in ZnSnO/SiGe-OI TFET with the Si back gate and have realized the n- and p-TFET operations in the single ZnSnO/SiGe TFET.

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References: [1] L. Lattanzio *et al.*, IEEE Elec. Dev. Lett. **33**, 167 (2012). [2] K. Kato *et al.*, Tech. Dig. IEDM 2017, p.377. [3] K. Kato *et al.*, SSDM 2018, p.187. [4] K. Kato *et al.*, Tech. Dig. EDTM 2019, SiDev2-1. [5] T. Tezuka *et al.*, Jpn. J. Appl. Phys. **40**, 2886 (2001). [6] K.-W. Jo *et al.*, Appl. Phys. Lett. **114**, 062101 (2019). [7] K. Kato *et al.*, Appl. Phys. Lett. **112**, 162105 (2018).

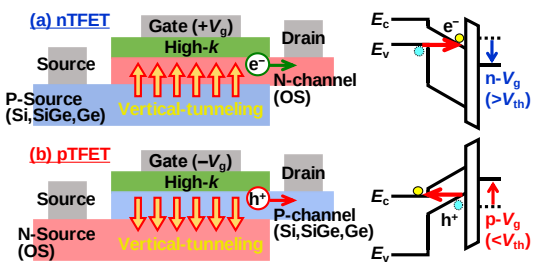


Fig. 1 Concept of (a) n- and (b) p- bilayer TFETs. In pTFET, negative V_g on p-channel generates holes at the channel surface after vertical BTBT, while positive V_g on n-channel generates electrons in nTFET.

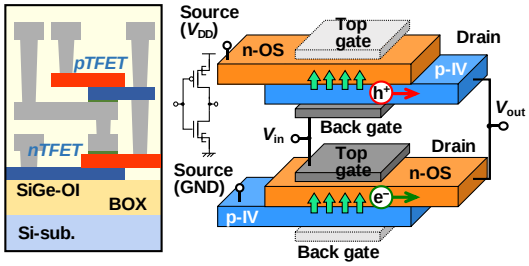


Fig. 2 Compact 3D-integration of n-/p- bilayer TFETs into CMOS circuit, by utilizing 3D stack SiGe-on-insulator and back gate technologies.

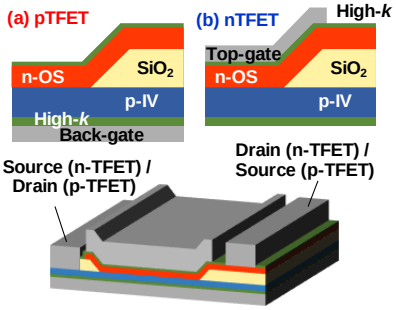


Fig. 3 Bilayer TFET structure of (a) pTFET and (b) nTFET for TCAD simulation.

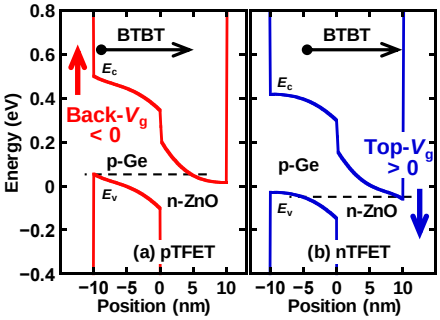


Fig. 4 (**Simulated**) Energy band diagram of the tunneling junction during (a) pTFET operation and (b) nTFET operation

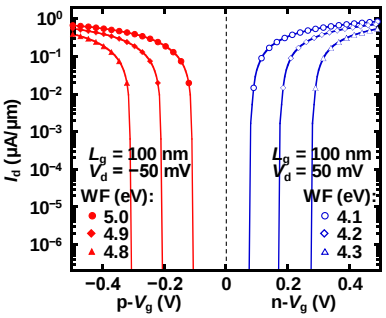
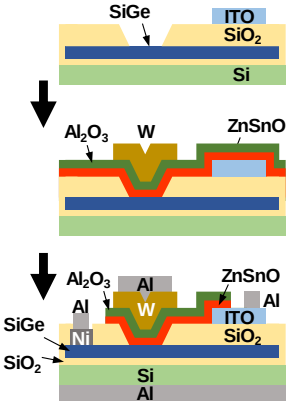


Fig. 5 (**Simulated**) I_d-V_g of pTFET (back-gate) and nTFET (top-gate) with various work functions.



- SiGe-on-insulator
  - *Ge condensation*
  - *SiGe thickness: 17 nm*
  - *BOX thickness: 25 nm*
  - *Ge fraction: 59%*
  - *Compressive strain: 1.8%*
- SiGe isolation
- SiO_2 deposition
- ITO formation
  - *Sputtering*
  - *N_2 anneal: 400℃*
- Tunnel window opening
- ZnSnO deposition
  - *Pulsed lased deposition (PLD)*
  - *Zn/Sn ratio in PLD target: 1.5*
  - *Temperature: 300℃*
  - *Thickness: ~12 nm*
- O_2 annealing: 400°C
- Top high-k deposition
  - *ALD-Al_2O_3: 1 nm*
  - *ECR-plasma oxidation*
  - *ALD-Al_2O_3: 9 nm*
  - *Thermal oxidation: 350℃*
- W top gate
- Al_2O_3 and ZnSnO pattern
- Ni source
- Al back gate
- Al contact pad
- PMA: 350°C

Fig. 6 Bilayer TFET device fabrication flow with n-ZnSnO and p-SiGeOI layers.

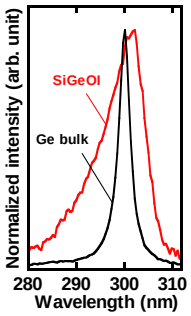


Fig. 7 Raman spectra of SiGeOI to evaluate Ge fraction.

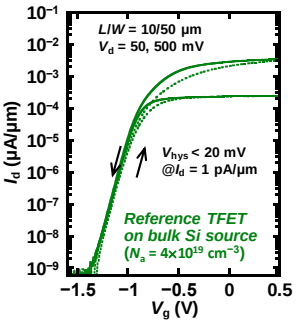
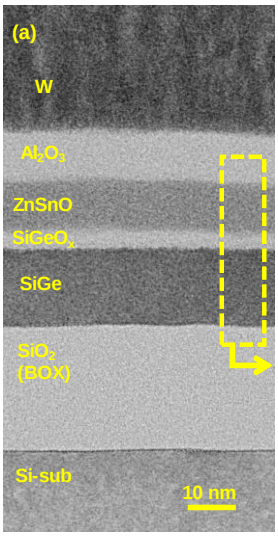
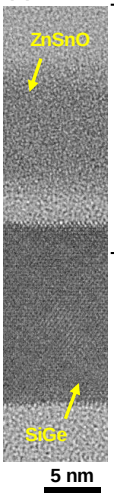


Fig. 9 I_d-V_g of reference ZnSnO/Si TFET fabricated on bulk Si source.





	p-TFET	n-TFET
p-SiGe	Channel	Source
n-ZnSnO	Source	Channel
Top W	(floating)	Gate
Back Al/Si-sub	Gate	(floating)
Ni	Drain M (< 0 V)	Source M (= 0 V)
ITO	Source M (= 0 V)	Drain M (> 0 V)

Fig. 8 Cross-sectional TEM images of n-ZnSnO/p-SiGe tunneling junction. Amorphous ZnSnO and single-crystal SiGe (Ge=59%) layers are observed.

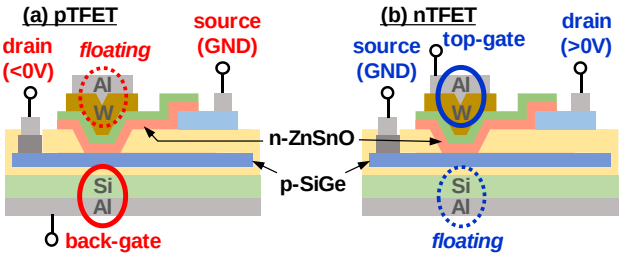


Fig. 10 Configurations of terminals for (a) pTFET and (b) nTFET demonstrations used in this study.

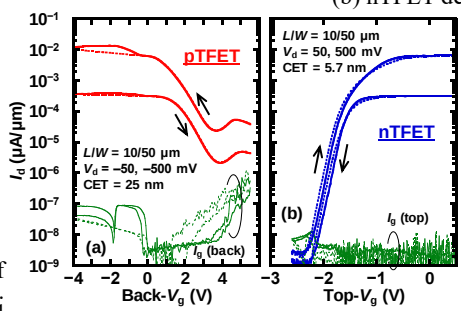


Fig. 11 (**Measured**) I_d-V_g of (a) p- and (b) n- TFETs.

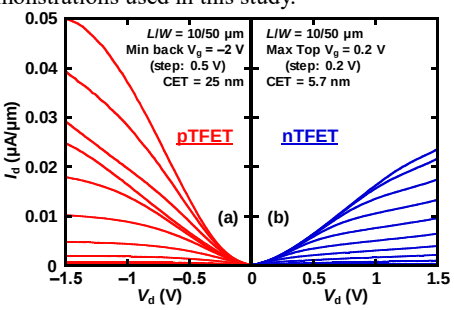


Fig. 12 (**Measured**) I_d-V_d of (a) p- and (b) n- TFETs.