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Recent progress in sequential 3D device stacking: Low temperature reliable top tier junction-less devices on 300mm wafers.

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Abstract

We report on recent development in the field of sequential 3D (S3D) device stacking. We show that some of the challenges of S3D can be circumvented by using junction-less top tier (planar or finfet) devices fabricated at low temperature (<525˚C) with reduced process complexity. Performance and reliability can be maintained despite the low thermal budget thanks to the junction-less device operation and the use of dipoles in the gate stack. 3D stacking of finfet devices at scaled design rules of 45nm fin pitch and 110nm gate pitch was demonstrated with lithography tight overlay (mean+3σ <15nm), enabling increased device density, without requiring further device dimensions scaling.

1. Introduction

S3D technology was first considered in the device roadmap for scaling purpose [1]. It was then envisioned as a solution for the beyond-silicon era to facilitate the co-integration of different channel materials such as Germanium and III-V materials [2]. More recently, at system level, partitioning of different functionalities into different tiers, also known as *functional scaling*, has driven much interest, to reduce form factor and to help co-integrate very different technologies, such as Logic and Radio-frequency [3]. Obviously, S3D integration scheme can bring benefits to both "More than Moore" and "More Moore applications". Such integration approach implies, however, significant adaptation of the device processing. In this context, we are reviewing the recent progress made in the integration of S3D device stacking and the optimization of the top tier device processing at low temperature.

2. Fabrication flow

Bottom tier bulk planar or finfet transistors are first processed on a *carrier* wafer, using a standard *"high temperature"* Replacement Metal Gate (RMG) process with direct metal contacts to the source and drain (S/D) (**Fig.1**). The finfets also feature an SADP fin patterning and embedded in-situ doped S/D epitaxy. After bottom tier processing up to the local interconnect layer(s), a planarization process is implemented, before wafer to wafer bonding, using a deposited oxide followed by chemical-mechanical polishing. Optionally, a SiCN dielectric can also be deposited for wafer to wafer dielectric bonding. A Silicon-on-insulator (SOI) *donor* wafer is then bonded to the carrier wafer to transfer a thin top crystalline silicon (c-Si) layer. For this purpose, the substrate of the SOI donor wafer is removed after bonding by grinding, Si dry etch and selective removal of the buried oxide by wet etch. The top device processing is then carried out at a low temperature, less than 525˚C, to minimize the impact on the bottom tier devices and metal interconnects. Alignment of the first processed top layer toward the last processed bottom laye is done by lithography through the thin top silicon layer and the bonding stack, in a 193nm immersion stepper. The top tier devices are inherently "SOI-like" and feature raised S/D with a Si:P and SiGe:B epitaxial process for the nMOS and pMOS, respectively. The top devices are junction-less featuring a constant doping in the channel and in the source and drain which is carried out by ion implantation and spike anneal activation, prior to the Si layer transfer by bonding, to avoid thermal impact on the bottom tier. 3D stacking of both planar [3] and finfet [4] devices was demonstrated with nanometric top to bottom tier alignment (**Fig.2** & **Fig. 3**).

3. Bonding requirements and thermal stability

The integrity of the top c-Si layer transfer is tightly linked to the bonding process. The bonding interface needs to be voids-free as well as thermally stable. This requires sufficient planarization of the patterned carrier wafer to reduce topography and avoid pattern-related voids (**Fig.4**). In addition, the thermal stability of the bonding interface can be ensured by applying a degassing anneal of the deposited bonding dielectric prior to bonding, with a minimum temperature corresponding to the one used in the top tier device processing (**Fig.5**).

4. Top tier device performance and reliability

I_D-V_G characteristics of the top tier devices exhibit good control of short channel effects and DC performance (**Fig.6a**). The threshold voltage, subthreshold slope and drain-induced barrier lowering (DIBL) vary with channel doping and channel thickness as expected from the junction-less operation (**Fig.6b & Fig.7**). A comparison between the top tier devices and devices processed on SOI wafers with the same low temperature flow, shows no significant difference in DC and RF performance, suggesting that the top silicon layer transfer has no significant impact on isolated devices (**Fig.8**). The low thermal budget of the top device processing precludes, however, any "reliability anneal" (>800°C), which impacts the quality of the gate dielectric. The use of $LaSiO_x$-based or Al_2O_3 interface dipoles [5] improve BTI reliability. The junction-less top devices also improve BTI reliability over inversion-mode devices thanks to their lower operating electric field [5,6]. When combining junction-less devices with $LaSiO_x$ dipole [5], the reliability target is met with considerable headroom and only ~0.1nm, for 0.2nm $LaSiO_x$ EOT penalty (**Fig.9**).

5. Conclusions

Recent results in 3D sequential integration demonstrate the potential of such a technology for both functional scaling and end-of-the-roadmap device scaling.

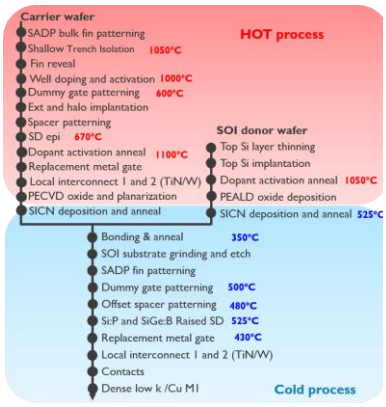

Fig. 1. Process flow of the 3D stacked finfets.

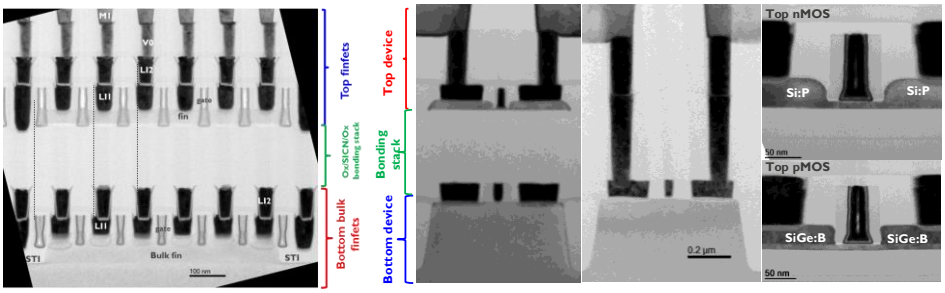

Fig. 2. TEM cross-section image of the fabricated 3D stacked finfets, along fins and across gates showing the tight alignment achieved by the top processed layers (Gate, Li1, Li2) toward the bottom layers.

Fig. 3. TEM cross-section of the 3D stacked planar devices (a) stacked top and bottom tier devices with nanometric alignment, (b) 3D contacts to the bottom devices and (c) magnified top tier P and NMOS devices.

References

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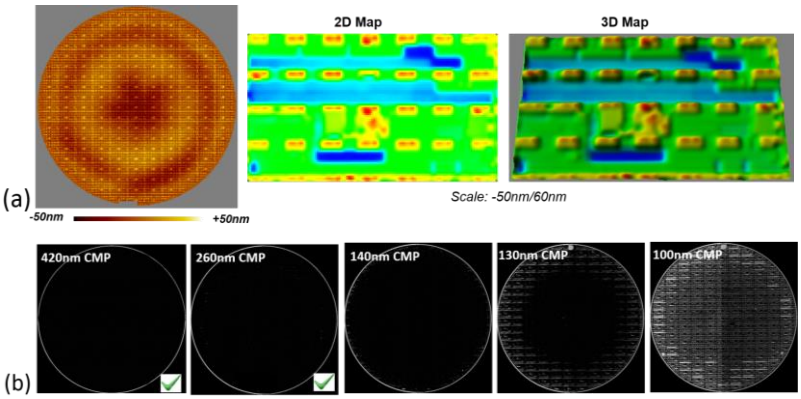

Fig. 4 (a) Patterned wafer geometry (PWG) of carrier wafer after full processing. Map of the nano-topography peak to valley value on full wafer and 2D and 3D plots at die level **(b)** High resolution Scanning acoustic microscope (HR SAM) images after wafer to wafer bonding of a blanket donor wafer onto the patterned carrier wafer processed with different amounts of planarization of the bonding oxide.

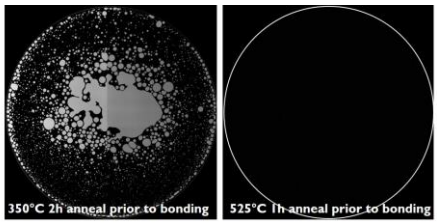

Fig. 5 HR Scanning acoustic microscope image after wafer bonding of a donor wafer onto a bottom carrier wafer, and a post bonding anneal at 525°C for 1h (mimicking the top device thermal budget). Degassing anneal before bonding is: 350°C 2h (left) and 525°C 1h (right).

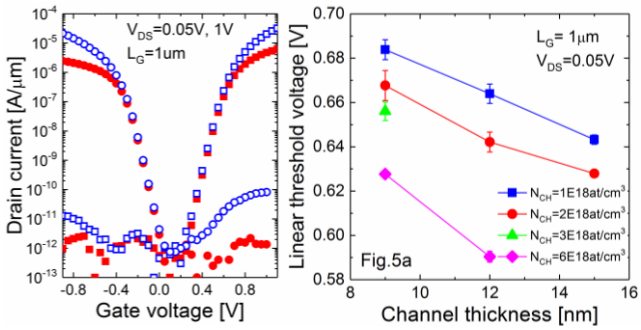

Fig. 6 (a) I_D-V_G of short channel top tier planar PMOS and NMOS devices in linear (V_{DS}=0.05V) and saturation (V_{DS}=1V) operation, **(b)** Threshold voltage dependence with channel thickness and channel doping in top tier NMOS devices.

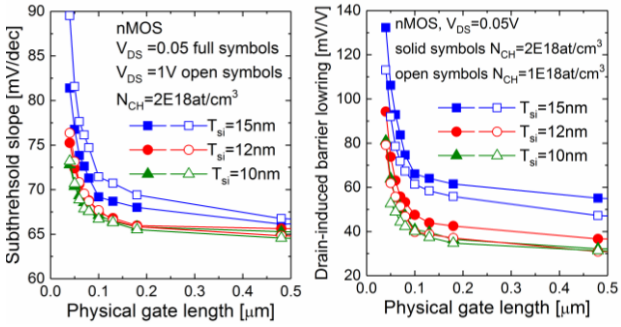

Fig. 7 (a) SS and **(b)** DIBL vs. L_G of top tier planar NMOS devices in linear (V_{DS}=0.05V) and saturation (V_{DS}=1V) operation for different channel thickness (10,12,15nm) and different channel doping (1, 2, 3E18at/cm^3)

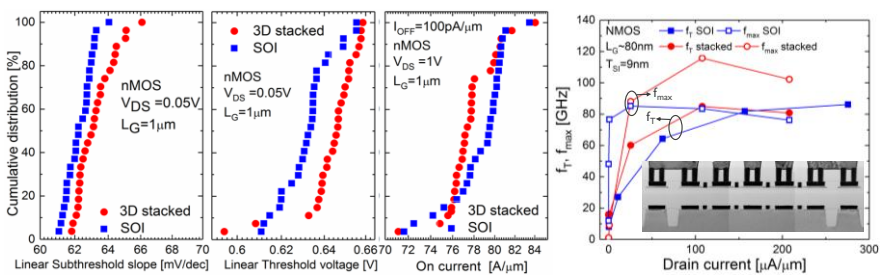

Fig. 8 (a) Cumulative distribution of SS, V_T, and I_{ON} comparing junction-less 3D stacked finfets and SOI finfets **(b)** f_T and f_{max} comparing junction-less 3D stacked and SOI planar devices. Inset TEM cross-section of the RF structure.

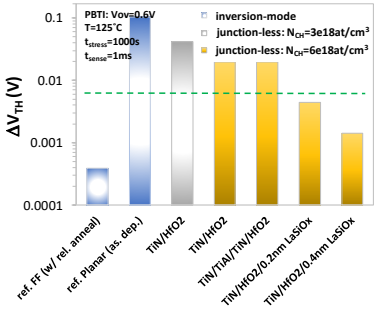

Fig. 9 PBTI V_{TH} shifts at for junction-less top tier finfets with various gate stacks and reference inversion-mode devices with and without reliability anneal.