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Bottom Tier High Voltage Device Thermal Stability in 3D Sequential Integration for More than Moore Applications

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Abstract
This paper analyses for the first time the maximum thermal budget (TB) that high voltage (5V) devices can sustain. Through comprehensive electrical characterization, it is shown that these devices can endure 500°C 5h anneal without any performance penalty nor process adaptation. As such TB is sufficient to process a high performance digital device on the top level, these results pave the way to a promising digital / high voltage analog devices partitioning in 3D sequential integration (3DSI) with the high voltage device being on the bottom level.

Introduction:

3DSI consists in stacking device layers in a sequential manner. This integration offers the highest 3D contact density [1] but comes at the cost of TB constraints for the top layer processing, in order to preserve the performance of the bottom one. 3DSI is a great candidate for More than Moore applications (Fig. 1), requiring High Voltages (HV) devices [2]. Previous studies have confirmed the stability of advanced digital top devices up to 500°C [3], and that TB is sufficient to process HP digital devices [4-5]. The main differences between HV and digital devices previously studied are summarize in Fig. 2. Digital advanced devices (0.9V) uses FDSOI technology with L_{gmin}=30nm, undoped channel and HfSiON/TiN gate stack. Meanwhile the HV MOSFET under study presents a doped BULK channel, SiO_2/Poly gate stack (EOT=13nm) and L_{gmin}=600nm. The aim of this paper is to evaluate the maximum thermal budget that can sustained HV MOSFETs used as bottom transistors of a 3DSI. For that purpose, additional TB (from 400°C to 600°C 2h) has been applied to BULK 5V devices (process flow and anneals split in Fig. 3).

Results:

Gate Stack Stability: The threshold voltage (V_{th}) for both N&P after the additional TB is stable up to 550°C 2h (Fig.4). However, a slight Vth shift of +45mV and +60mV starts to be observed at 600°C 2h, for N&P respectively. Given that the channel doping is stable (Fig. 5) and in the absence of metal gate, the V_{th} increase is explained by a deactivation of the polysilicon dopants. Indeed, the flatband voltage (V_{fb}) is reduced by ~60mV at 600°C 2h (Fig. 6), in agreement with the V_{th} shift. Thanks to C-V quantum mechanical model, the poly doping concentration is estimated to 10^{20} at/cm^{-3} for the reference wafer (Fig. 7) while it is decreased at 600°C 2h to 5.10^{19} (Fig. 8) for N&P. Furthermore, the unsilicided polysilicon resistance (Fig. 9) also shows an increase with the TB, but only deactivation at the SiO_2 interface impacts the Vth.

***Access Resistance Stability*:** Full sheet resistance measurements were performed in order to compare the activation level on S/D regions gate regions (Fig. 9). For the unsilicided crystalline structures, the sheet resistance does not present any major degradation. In contrast, the gate resistivity is degraded up to 70% at 600°, effect more pronounced on NMOS. This shows that dopant deactivation is higher on polycrystalline than on crystalline regions. It should be noted that, as previously seen, this gate deactivation has only a small effect on V_{th} (visible only at 600°C 2h), which can be compensated by adjusting the channel doping.

The silicided S/D resistance, is stable for NMOS and even improves for PMOS (Fig. 10). In addition, no impact on junction leakage has been observed highlighting good silicide stability (Fig. 11) [6]. However, a silicided polysilicon resistivity degradation is observed starting at 550°C 2h, which could be an indication of NiPt agglomeration on poly regions. Thus the TB must be kept at 500°C 5h to preserve the gate resistance.

***Global performance stability*:** The I_{on}/I_{off} of N&P are stable despite the TB (Fig. 12), and so is the voltage gain gm/ID (Fig. 13) for N&P (PMOS not shown here). Similarly, the effective mobility measured on long channel devices (Fig. 14) is also unaffected. The access resistance extracted using the R_{tot} method (Fig. 15) does not show any degradation. This can be explained by the fact that in a long channel device, the R_{access} becomes negligible in comparison to the channel resistance. Overall, device performance is ensured even for the higher TB of 600°C 2h.

Conclusions: For the first time, the thermal stability of high voltage BULK devices is quantified. It is shown that static figure of merit are unchanged up to 600°C 2h TB. A slight poly deactivation is observed for the highest TB (600°C 2h) affecting only the gate WF (no additional poly depletion) and can be compensated for by modifying the channel dopant concentration.

The silicide stability on the source and drain is shown to be stable, the weak point relying only in the silicide instability of poly gate starting from 550°C post anneals. Therefore, the TB must be kept below 550°C 2h in order to ensure stable dynamic performance. These results shows that high voltage SiO_2/ Poly devices can be integrated on the bottom level of 3DSI with a comfortable TB (at least 500°C 5h) to process the top device.

Acknowledgements: This work was partly funded by Nano 2022 and 3DMUSE H2020 project.

References: [1] L. Brunet *et al.,* VLSI 2016 [2] P. Batude *et al.,* IEDM 2017 [3] C. Fenouillet *et al.,* EESDERC 2014 [4] L. Pasini *et al.,* VSLI 2016 [5] C.-M. V. Lu *et al.,* VLSI 2017 [6] T. Yamaguchi *et al.,* IEDM 2010

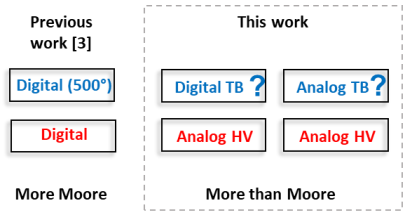

Fig. 1. Description of this work objective: quantify the maximum TB sustainable by HV Analog device for more than Moore applications.

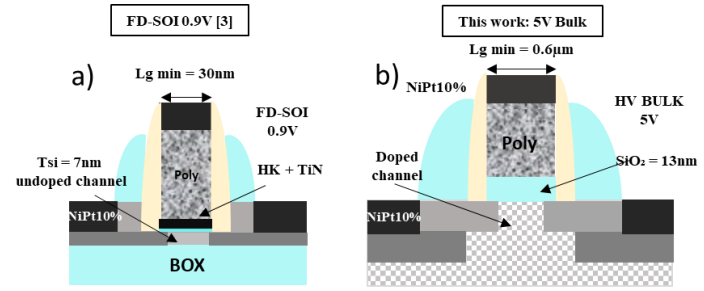

Fig. 2. Schematic of the a) advanced digital (0.9V) FD-SOI technology studied in [3] compared to the 5V BULK adapted to sensing applications.

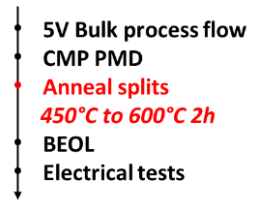

Fig. 3. Process flow and anneal splits.

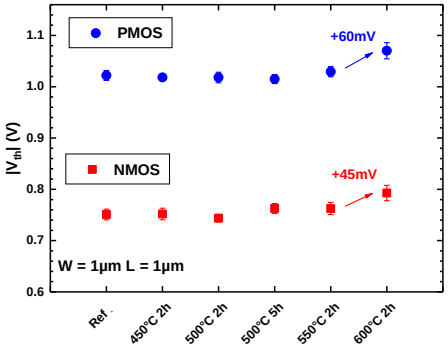

Fig. 4. Threshold voltage of NMOS and PMOS extracted by constant current method versus TB.

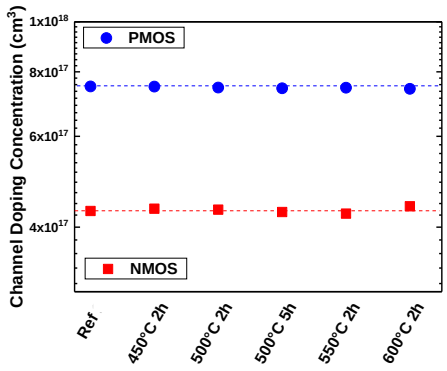

Fig. 5. Channel doping concentration extracted by back-bias sensitivity of NMOS and PMOS.

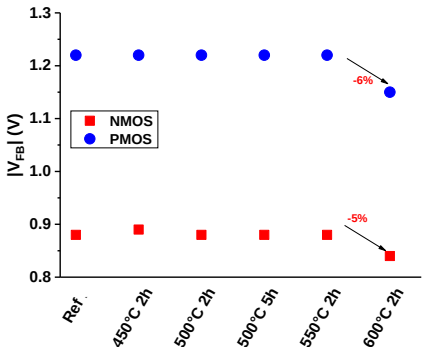

Fig. 6. Flatband voltage extracted by $1/C^2$ method of NMOS and PMOS.

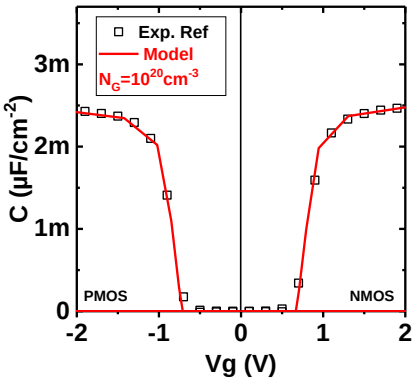

Fig. 7. Gate doping concentration of Reference wafer estimated with QM model.

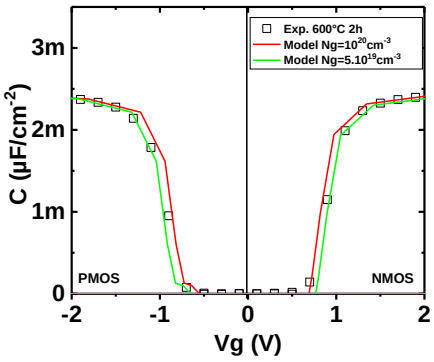

Fig. 8. Gate doping concentration for TB 600°C estimated with QM model using a cte doping constant profile.

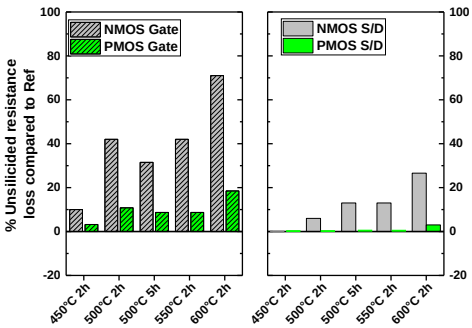

Fig. 9. Unsilicided resistance loss in % with respect to reference for N&P.

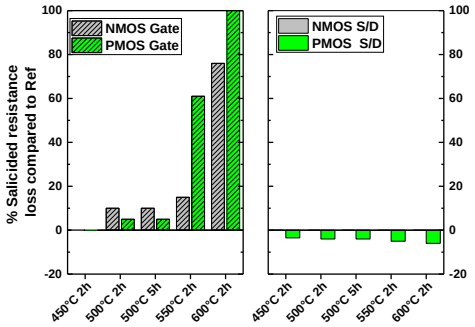

Fig. 10. Silicided resistance loss in % with respect to reference for N&P.

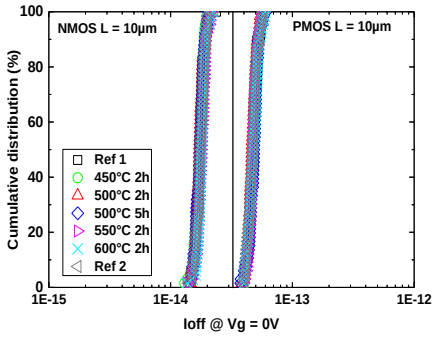

Fig. 11. Cumulative probability of I_{off} of NMOS and PMOS for 130 devices.

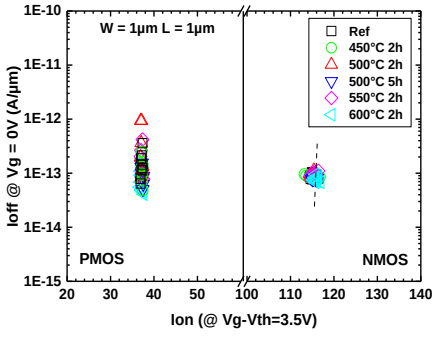

Fig. 12. NMOS I_{on}/I_{off} tradeoff versus thermal anneals. L = 3, 1µm. V_{dd} = 5V.

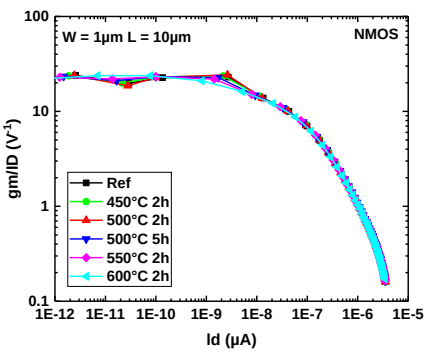

Fig. 13 NMOS voltage gain. L = 10µm.

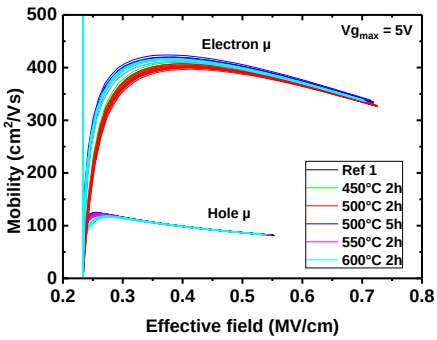

Fig. 14 Effective mobility of NMOS and PMOS versus anneals. L = 10µm.

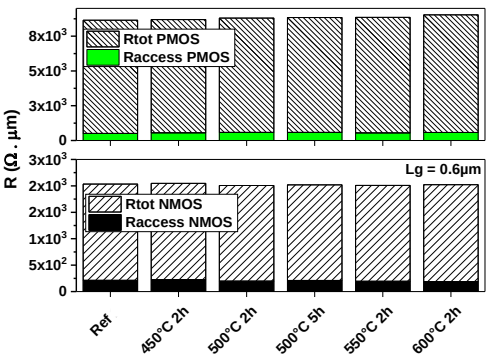

Fig. 15 Total and access resistance of NMOS and PMOS. L_{gmin} = 0.6µm.