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Effects of hydrogen ion implantation dose on electrical and physical properties of (100) and (111) Ge-on-insulator substrates fabricated by Smart-cut process

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Abstract

We examine the influence of hydrogen ion implantation (I/I) dose on the properties of 2-inch (100) and (111) Ge-on-insulator (GOI) wafers fabricated by the smart-cut process. The high I/I dose of 1×10^{17} cm^{-2} causes the slight degradation of GOI quality in terms of the mobility. On the other hand, defect-less (100) and (111) GOI substrates can be realized with the low I/I dose of 4×10^{16} cm^{-2}.

1. Introduction

GOI structures have received much attention for scaled MOSFETs because of their high carrier mobility and compatibility with the Si CMOS platform [1, 2]. Here, formation of high quality GOI structures is a key. The Smart-cut technology has widely been used to fabricate high-quality GOI structures [3]. In the previous works, we studied the annealing effect on the quality of GOI films fabricated by the smart-cut process [4, 5]. However, the effect of the I/I dose on the GOI quality in the smart-cut process has not been reported yet. In this work, the influence of hydrogen I/I dose in (100) and (111) GOI layers fabricated by smart-cut technology was systematically studied in terms of physical and electrical characteristics at various annealing temperatures.

2. Experiments

The smart-cut process used in this study was shown in Fig. 1. 2-inch (100) and (111) bulk p-Ge wafers were used to fabricate the GOI substrates. After pre-cleaning, a 100-nm-thick SiO_2 sacrificial layer was deposited on the Ge wafers. Then, the H^+ implantation process was carried out with an energy of 80 keV and two dose conditions, 1×10^{17} cm^{-2} and 4×10^{16} cm^{-2}. After removing the SiO_2 layer, Al_2O_3/GeO_x layers were formed using a plasma pre-oxidation method to improve the interface property [6]. Then, bonding of the Al_2O_3/GeO_x/Ge wafer with a 4-nm-thick Al_2O_3/2-μm-thick SiO_2/Si wafer was performed in a manual way. The bonded wafers with the high I/I dose were split by annealing at 400 °C for 3 hours, while the bonded wafers with the low I/I dose were split by annealing at 400 °C for about 48 hours. Subsequently, chemical mechanical polishing was carried out for surface planarization. Finally, fabricated GOI samples were annealed at different temperatures to improve the quality of GOI layers.

Hall bar devices were fabricated on the annealed GOI substrates. The GOI layers were patterned by reactive ion etching system. The 10-nm-thick Al_2O_3/GeO_x layers were formed by plasma pre-oxidation for passivation. After contact hole formation, a 150-nm-thick Ni layer was deposited by sputtering. Fig. 2 shows the fabrication flow and the schematic view of the fabricated Hall bar device, which were also used as back-gate type GOI pMOSFETs to evaluate the GOI quality near the bonding interface.

3. Results and Discussion

Raman analyses were conducted to evaluate the physical properties and the crystallinity of the GOI layers with the high and low I/I dose conditions. Fig. 3(a) and (b) show the Raman spectra of the as-fabricated (100) and (111) GOI samples. For both surface orientations, the Raman spectra of the high dose GOI were broader than those of the low dose ones, suggesting the higher damages in the high dose GOI. After annealing at 550 °C, all the GOI substrates show the similar Raman spectra to that of bulk Ge, as shown in Fig. 3(c) and (d), indicating the improvement of crystallinity. Fig. 4(a) and (b) show the FWHM values for the (100) and (111) GOI samples, respectively. Even after annealing, the high dose GOI samples have higher FWHM than the low dose one, suggesting that the damages generated in the I/I process still remains after annealing at 550 °C. Fig. 5 shows the strain values in the GOI layers evaluated from the Raman shift of the Ge peak. The higher tensile strain was observed in the higher I/I dose GOI substrates. These high strain values in the high dose GOI might be due to the effect of remaining defects [8, 9]. Also, the (111) GOI substrates with the high dose show the higher tensile strain than the (100) ones, attributable to the difference in the effect of defects between the (111) and (100) layers [10]. Meanwhile, the GOI substrates with the low I/I dose exhibit tensile strain of 0.1-0.2 % regardless of surface orientation, which is consistent with our previous results [4]. This amount of tensile strain can be explained by the difference in the thermal expansion coefficient between Ge and SiO_2 [7].

The carrier (hole) density (Fig. 6) and the Hall mobility (Fig. 7) were evaluated from the Hall measurements. The GOI samples annealed at 550 °C show the lowest hole density, which is identical to that in the initial bulk Ge wafers, for both the high and low dose conditions. The highest hole mobility for annealing at 550 °C confirms us that this annealing temperature is optimum and that the annealing at 600 °C can induce any thermal damages [5]. On the other hand, the GOI substrates with the low I/I dose show the higher hole mobility than those with the high I/I dose, indicating the better GOI quality for the low I/I dose even after annealing at 550 °C. The mobility values at 550 °C are close to the bulk Hall mobility at the similar hole concentrations (2300-2100 cm^2/Vs) [11], suggesting that most of the generated defects are recovered through the annealing process. Fig. 8 show the transfer characteristics of the back-gate GOI pMOSFETs. The GOI pMOSFETs show the similar electrical properties between (100) and (111) GOI, irrespective of the I/I dose condition, suggesting that there are almost no damages near the bonded interfaces. Fig. 9 shows the effective mobility of the (100) and (111) GOI pMOSFETs. All the pMOSFETs show the high effective mobility of ~350 cm^2/Vs, indicating the good quality of the fabricated GOI structures.

4. Conclusions

The influence of the hydrogen I/I dose on the properties of (100) and (111) GOI layers fabricated by the smart-cut process was studied. The high I/I dose of 1×10^{17} cm^{-2} caused the slightly low crystallinity and electrical characteristics even after the annealing at the optimum temperature. The high tensile strain of 0.3-0.4 % was observed in GOI with the high I/I dose. The high Hall and effective mobility has promised the high quality of (100) and (111) GOI wafers with the low I/I dose of 4×10^{16} cm^{-2}.

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References [1] W. Wu et al., IEEE Electron Device Lett. **39** (2018) 176. [2] Z. Zheng et al., Appl. Phys. Lett. **109** (2016) 023503. [3] M. Kim et al., Semicond. Sci. Technol. **33** (2017) 015017. [4] J. Kang et al., Mat. Sci. Semicon. Proc. **42** (2016) 259. [5] C. M. Lim et al., Electron Devices Technology and Manufacturing (2019) 232. [6] M. Ke et al., IEEE J. Electron Devices Soc. **6** (2018) 950. [7] M. Veerappan et al., Semicond. Sci. Technol. **32** (2017) 035021. [8] T. Akatsu et al., Appl. Phys. Lett. **86** (2005) 181910. [9] S. K. Gautam et al., J. Appl. Phys. **115** (2014) 143504. [10] Y. L. Chao et al., Jpn. J. Appl. Phys. **45** (2006) 8565. [11] O. A. Golikova et al., Sov. Phys. Solid State **3** (1961) 10.

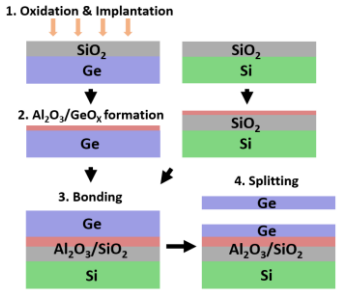

Fig. 1 Smart-cut process flow for the GOI substrate.

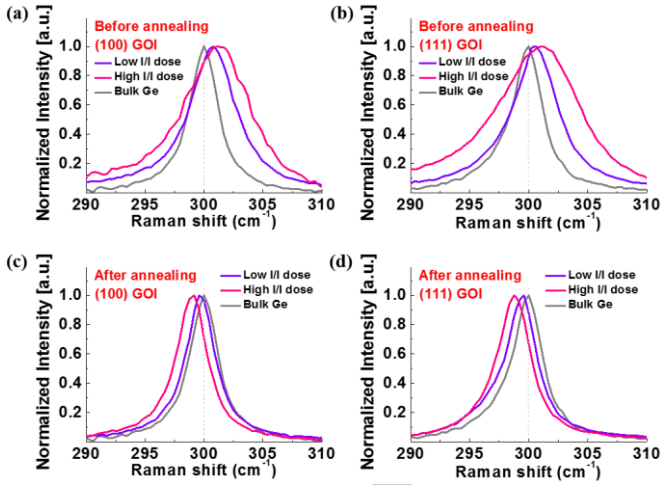

Fig. 3 Raman spectra of SC (100) and (111) GOI substrates before and after annealing at 550 °C with two kinds of H^+ I/I dose conditions.

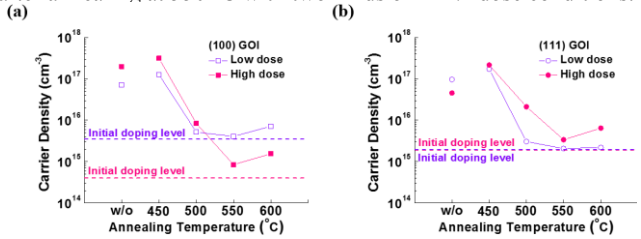

Fig. 6 Hole density depending on different I/I dose conditions for (a) (100) and (b) (111) GOI substrates.

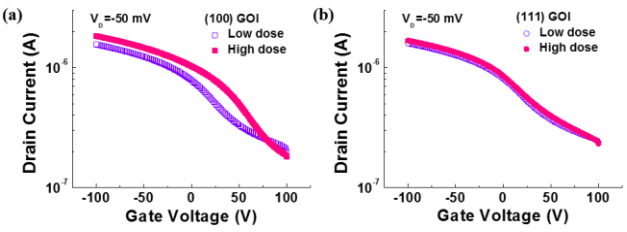

Fig. 8 I_D-V_G curves of fabricated (a) (100) and (b) (111) GOI pMOSFETs depending on I/I dose conditions.

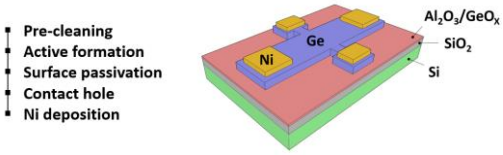

Fig. 2 Schematic diagram of Hall bar devices (back-gate type pMOSFETs).

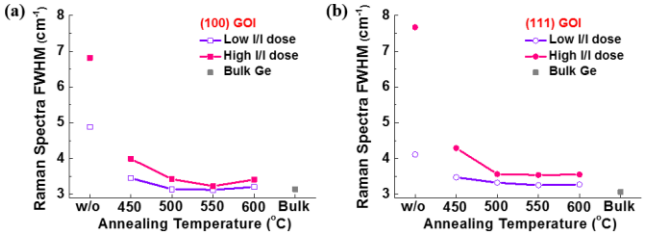

Fig. 4 FWHM values of high and low I/I dose GOI samples at various temperatures for (a) (100) and (b) (111) surface orientation.

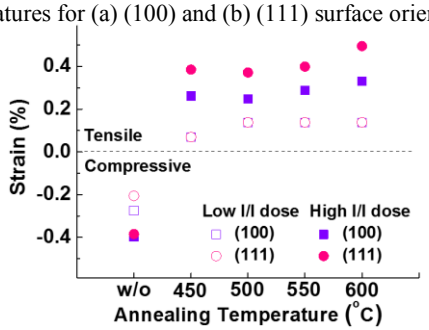

Fig. 5 Strain values in (100) and (111) GOI layers for different I/I dose conditions.

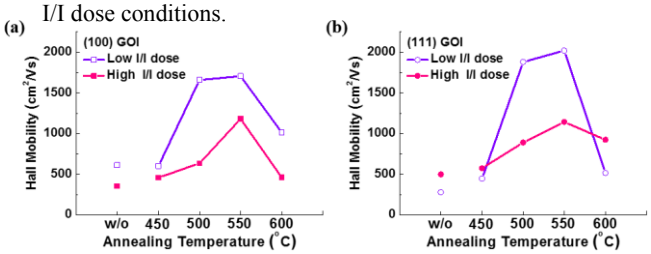

Fig. 7 Hall hole mobility depending on different I/I dose conditions for (a) (100) and (b) (111) GOI substrates.

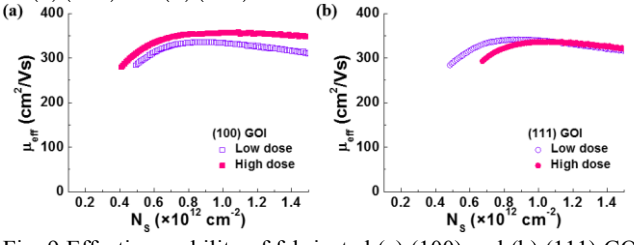

Fig. 9 Effective mobility of fabricated (a) (100) and (b) (111) GOI pMOSFETs depending on I/I dose conditions.