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Accurate evaluation of contact resistivity between InAs/Ni-InAs alloy

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Abstract

A Ni-InAs source/drain (S/D) nMOSFET is one of promising future logic devices. In this study, contact resistivity ρ_{int} between InAs and Ni-InAs are evaluated by novel TLM (transmission line method) patterns on InAs-OI (InAs-On-Insulator), for the first time. Since conventional TLM patterns are not adequate to evaluate the low contact resistivity with high accuracy, we proposed a new TLM pattern which can include multiple Ni-InAs/InAs contacts. The high accuracy measurement of ρ_{int} is demonstrated by combining InAs-OI structures with this TLM. The evaluated ρ_{int} of 3.0×10^{-8} Ωcm^2 is found to be in good agreement with the theoretical lower limit.

1. Introduction

Metal source/drain (S/D) is one of promising S/D structures of InGaAs (InAs) nMOSFETs because of the implantation free formation at low temperature [1]. It has already been reported that metal-In(Ga)As alloys like Ni-InGaAs and Ni-InAs can realize an ultra-shallow and steep junction [2, 3]. These properties are suitable for future logic device structures such as 3-dimensional vertically-stacked CMOS [4]. Here, the contact resistance in S/D is becoming the more serious problem with scaling, because of the limited contact area. The reported contact resistivity, ρ_{int}, between InGaAs and Ni-InGaAs is still relatively high because of the non-zero Schottky Barrier Height (SBH) [1, 2]. On the other hand, ρ_{int} between InAs and Ni-InAs is expected to be very low because no SBH at metal/InAs interfaces is suggested [5]. However, there is no report on experimental evaluation of ρ_{int} between InAs and Ni-InAs, because of the complicated resistance components in Ni-InAs/InAs grown on bulk III-V.

In this study, we propose a new TLM test pattern allowing to evaluate ρ_{int} with high accuracy even of for the very low values. Here, InAs-OI structure is utilized to simplify the resistance components. As a result, ρ_{int} in Ni-InAs/InAs with the electron density of 2×10^{18} cm^{-3} is evaluated as 3×10^{-8} Ωcm^2, which is almost the same value as the theoretical limit under SBH of 0 eV.

2. Proposal of new evaluation scheme of ρ_{int}

The parasitic resistance components in Ni-InAs S/D are shown in Fig. 1. Here, TLM patterns to measure each resistance component are shown in Fig. 2. The contact resistance R_{int} is determined by the junction structure, the current flow and contact resistivity ρ_{int}. Here, it is difficult to accurately evaluate ρ_{int} in the conventional structures of Ni-InAs junctions with InAs, grown on III-V substrates (Fig. 2(b)), because it is hard to quantify the interface area through which the current passes in the InAs/Ni-InAs junctions. In contrast, Ni-InAs formed on thin InAs-OI substrates allows us to provide the accurate interface area, as shown in Fig. 2(d), and, as a result, ρ_{int} can be simply determined by R_{int} x d, where d is the thickness of the InAs-OI layer.

On the other hand, the measurement accuracy of ρ_{int} is insufficient in conventional TLM patterns even for InAs-OI, because R_{int} is much lower than the sheet resistance of InAs and the total parasitic resistance R_{ext} in Fig. 1. Thus, we propose a series of new TLM patterns, shown in Fig. 3, to improve the accuracy. Here, the multiple regions of InAs and Ni-InAs are formed between the two metal contacts. When the number of the InAs channel regions included between the two terminals for monitoring the voltage drop is defined as the number of the InAs regions N, R_{ext} is expressed by $N \times (L_{sp}R_{Ni-InAs} + 2R_{int})$, where L_{sp} is the spacer length of Ni-InAs and, thus, is proportional to N. This is because the two Ni-InAs/InAs interfaces are included per one InAs channel region. Since $R_{Ni\text{-}InAs}$ is evaluated by the TLM pattern of Fig. 2(c), R_{int} can be accurately determined from the slope of the R_{ext}-N plot. Note here that is independent of R_{mc} and the slope is robust against a variation of measured R_{ext}. Table 1 summarizes the features of each TLM structure in terms of the evaluation accuracy of ρ_{int}. The TLM scheme including the new pattern can provide the best accuracy.

3. Experiments and Results

The fabrication process flow of the TLM patterns on (111) InAs-OI is shown in Fig. 4. 50-nm-thick (111)B InAs-OI substrates with the electron density of 2×10^{18} cm^{-3} were fabricated by the Smart Cut method, as we have reported in [6]. 10-nm-thick Al_2O_3 was deposited by ALD, followed by 30-nm-thick Ni deposition by EB evaporation. Ni-InAs was formed by RTA at 250 ºC for 1 min, followed by selective etching of unreacted Ni by HCl. Finally, Ti/Pt contact pads were formed by a lift-off process. Fig. 5 (a), (b) and (c) are the prepared TLM patterns correspond to Fig. 2(c, d) and Fig. 3, respectively. The measured TLM resistance of 50-nm-thick Ni-InAs is shown in Fig. 6. The sheet resistance of Ni-InAs, $R_{Ni\text{-}InAs}$, is 21.4 Ω/sq and the resistivity is 107 μΩcm, which is half of that of Ni-InGaAs [1]. The resistance measured with new TLM patterns as a function of the number of the InAs regions N and the total spacing gap length of the InAs-OI channel is shown in Fig. 7(a). Also, the external resistance R_{ext}, which is the R-axis intercept of R-L graph, as a function of N is shown in Fig. 7(b). Good linearity is shown and the slope of $R_{\mathrm{ext}} - NL_{sp}R_{\mathrm{Ni-InAs}}$ corresponds to $2R_{int}$. The evaluated ρ_{int} values with conventional TLM and new TLM are shown in Fig. 8. The values by conventional TLM have large variation. On the other hand, new TLM provides the high accuracy ρ_{int} value of 3.0×10^{-8} Ωcm^2, which is in good agreement with the theoretical lower limit between metal and InAs with an electron density of 2×10^{18} cm^{-3}, determined by a Hall measurement, under SBH of 0 eV. This result suggests that the contact with no Schottky barrier can be realized for Ni-InAs/InAs.

4. Conclusions

We proposed the new TLM patterns allowing to evaluate the low contact resistivity with high accuracy and demonstrated the effectiveness for the Ni-InAs/InAs-OI contact. The contact resistivity ρ_{int} between Ni-InAs and InAs has been in good agreement with the theoretical lower limit with SBH of 0 eV, indicating that InAs is promising for metal S/D MOSFETs with extremely-low parasitic resistance.

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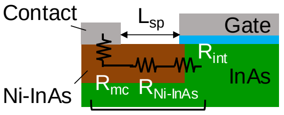
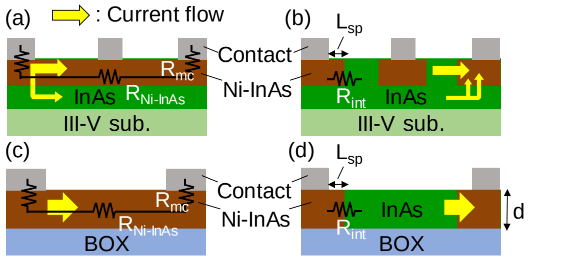


$$R_{ext} = R_{mc} + L_{sp} \times R_{\mathrm{Ni-InAs}} + R_{int}$$

Fig. 1 Schematic view of parasitic resistance of an InAs MOSFET with Ni-InAs S/D. R_{mc} is the contact resistance between a metal and Ni-InAs. $R_{Ni\text{-}InAs}$ is the sheet resistance of Ni-InAs. R_{int} is the contact resistance between Ni-InAs and InAs, which is determined by the junction structure and contact resistivity ρ_{int} between Ni-InAs and InAs.



$R_{ext} = R_{mc}$ $\quad$ $R_{ext} = R_{mc} + L_{sp} \times R_{\mathrm{Ni-InAs}} + R_{int}$

Fig. 2 TLM patterns to measure the parasitic resistance of Ni-InAs S/D. (a, b) An InAs layer is grown on a III-V substrate. (c, d) An InAs layer is on an insulator. (a, c) Ni-InAs is formed over the entire surface on InAs to measure the R_{mc} and $R_{Ni\text{-}InAs}$. (b, d) Ni-InAs is partly formed in InAs-OI to measure the R_{int}.

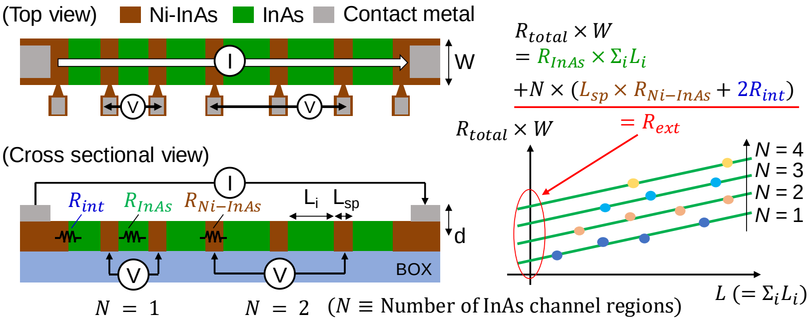


Fig. 3 A top and a cross-sectional view of a new proposed TLM pattern are shown. The intercept on the R-axis in the plot of resistance as a function of the spacing gap L increases linearly with an increase in the number of the InAs channel regions between two metal contacts N, as shown in the formula.

Table 1 Comparison of each structure in terms of evaluation accuracy of the contact resistivity ρ_c and ρ_{int}, and the sheet resistance $R_{Ni\text{-}InAs}$.

Structure	R_c , ρ_c (Metal/Ni-InAs)	$R_{Ni\text{-}InAs}$ (Ni-InAs)	R_{int} , ρ_{int} (Ni-InAs/InAs)
TLM on III-V sub.	△	○	×
TLM on InAs-OI	○	◎	△
New TLM on InAs-OI	○	◎	○

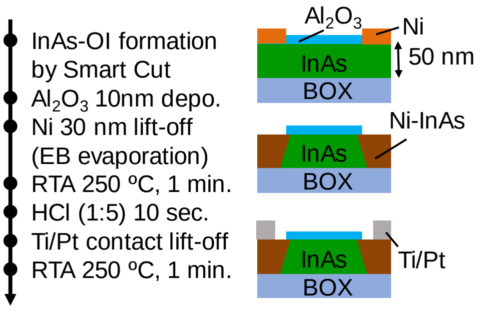


Fig. 4 The fabrication process flow of TLM patterns and Hall Bar on (111) InAs-OI.

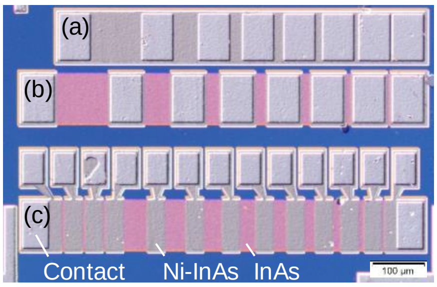


Fig. 5 Optical microscope images of TLM patterns of (a) Ni-InAs (Fig. 2 (c)) and (b) InAs (Fig. 2 (d)), and (c) new TLM patterns (Fig. 3).

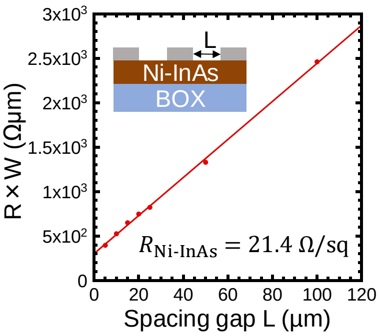


Fig. 6 Measured TLM resistance of Ni-InAs as a function of the spacing gap.

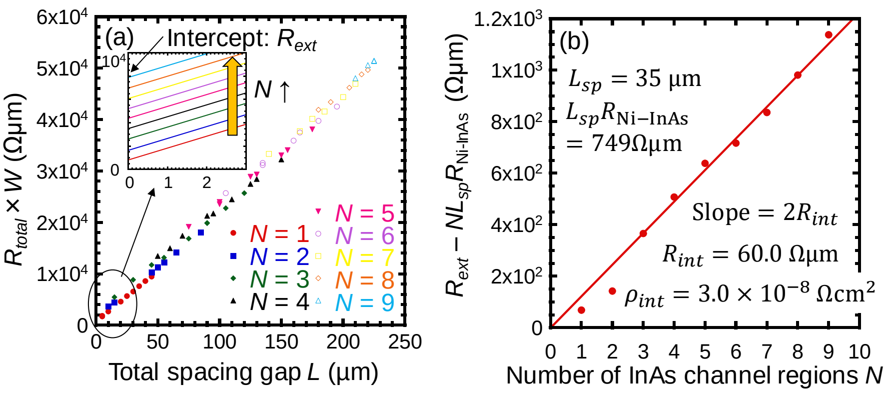


Fig. 7 (a) Measured resistance of new TLM versus the total length of the InAs channel as a parameter of the number of the InAs regions. (b) Intercept R_{ext} values on the R-axis in (a) as a function of the number of the InAs regions. The value of the vertical axis is taken to be $R_{ext} - NL_{sp}R_{Ni-InAs}$, where L_{sp} is 35 μm, and $R_{Ni\text{-}InAs}$ is 21.4 Ω/sq measured in Fig. 6. The slope of this graph corresponds to $2R_{int}$.

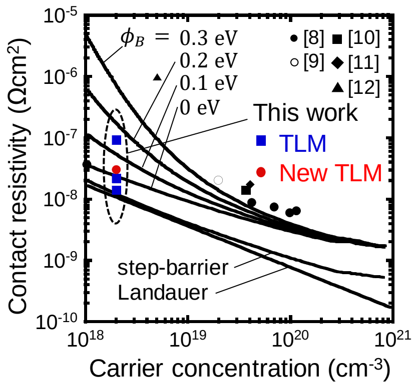


Fig. 8 Summary of contact resistivity between metals and n-InAs as a function of the electron concentration. Solid lines show the theoretical values as a parameter of SBH, reported in [7].