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The Impact of Stress and Parasitic RC in Sub-40nm MF and MR nMOSFETs for RF and mm-wave CMOS Applications

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Abstract

Multi-finger (MF) and multi-ring (MR) nMOSFETs were designed and fabricated in 40nm CMOS technology to explore the layout dependent stress, effective mobility (μ_{eff}), and parasitic RC responsible for high frequency performance. For the first time, the experimental proves the advantages of MR nMOSFETs, such as the increase of μ_{eff}, driving current (I_{DS}), and transconductance (g_m), and smaller parasitic source resistance (R_S), all of which are in favor of high speed and high frequency design. However, the undesired increase of 3-D fringing capacitances emerges as a critical trade-off influencing high frequency performance. In this paper, comprehensive analysis of the layout dependent effects and underlying mechanisms can facilitate the nanoscale devices layout optimization in the right direction for RF and mm-wave CMOS circuits design and applications.

I. Introduction

MF devices have been widely used in RF and analog circuits design attributed to the effective reduction of gate resistance (R_g). However, the smaller finger width (W_F) associated larger finger number (N_F) aimed at sufficiently low R_g, may lead to the penalties, such as g_m degradation due to lower μ_{eff} caused by STI compressive transverse stress $\sigma_\perp$ and larger R_S from longer source line, and the increase of gate capacitance (C_{gg}) originated from the gate sidewall and finger-end fringing capacitances (C_{of} and $C_{f(poly-end)}$) [1]-[4]. All of the mentioned factors result in significant impact on high frequency performance like f_T and f_{MAX}. In this paper, a new device layout, namely multi-ring (MR) MOSFET is proposed as a potential solution to reach higher μ_{eff} and improvement of g_m. The basic idea is that STI compressive $\sigma_\perp$ can be minimized in the MR layout due to miniaturized STI area around two ends of the gate finger. As for the ultimate goal of higher f_T and f_{MAX}, the parasitic RC like C_{of}, $C_{f(polyend)}$, and R_S appear as critical parameters deserving extensive investigation to explore a complete spectrum of the layout dependent effects and optimization guideline for RF performance enhancement.

II. MF and MR nMOSFETs Layout and Fabrication

MF and MR nMOSFETs were fabricated in 40nm CMOS technology with 40nm drawn length and $T_{ox(inv)}$=1.95nm. Fig.1 (a)~(b) illustrate the MF layouts with various W_F and N_F at fixed $W_F \times N_F = W_{tot}$=32μm. Note that the smaller W_F and larger N_F for lower R_g may lead to lower μ_{eff} due to increased STI compressive $\sigma_\perp$. Thus, MR MOSFET shown in Fig. 2(a)~(b) with various W_F and ring number (NR, N_F=4*NR) are proposed to effectively suppress the STI compressive $\sigma_\perp$ attributed to very small STI area near two ends of every gate finger.

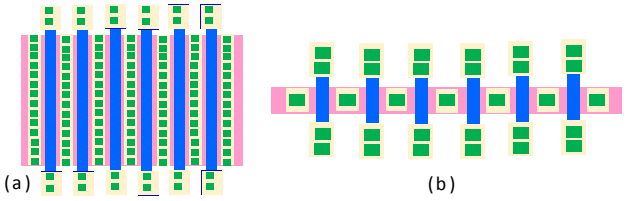

Fig. 1 Schematics of MF nMOS layouts with various W_F and N_F at fixed $W_F \times N_F$=32μm (a) W2N16 (b) W025N128.

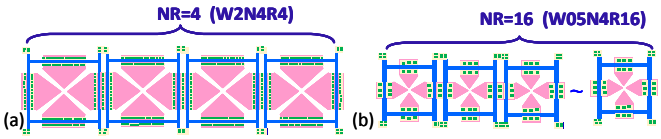

Fig.2 Schematics of MR nMOS layouts with various W_F, N_F, and NR at fixed $W_F \times N_F \times NR$ =32μm (a) W2N4R4 (b) W05N4R16.

III. Layout Dependent Effects in DC and High Frequency Characteristics – MF and MR nMOSFETs

Fig. 3 (a) presents the source line routing with contacts to source/drain for MF MOSFET, which suggests significant increase of R_S in case of very large N_F. Fig. 3 (b) shows the R_S vs. N_F determined by our proprietary matrix method in which the MR nMOS can achieve much smaller R_S than MF nMOS at the same N_F and W_F due to wider metal width and more contacts in parallel allowed in MR layout. More interestingly, the threshold voltage in linear and saturation regions, V_{Tlin} and V_{Tsat} vs. W_F shown in Fig. 4(a) and (b) indicate obvious inverse narrow width effect (INWE) for MF nMOS whereas some abnormal trend for MR nMOS, such as INWE in V_{Tlin} vs. W_F but narrow width effect (NWE) in V_{Tsat} vs. W_F . Moreover, MR nMOS reveal apparently lower V_{Tlin} and V_{Tsat} than MF nMOS and particularly large drop in case of W_F=2μm. It appears as a new observation and suggests different channel dopant concentrations in MF and MR nMOS, due to the difference in the compressive stress induced retardation of boron diffusion [5]. For MR nMOS with smaller compressive $\sigma_\perp$, thus less retardation, i.e. faster boron diffusion may lead to lower boron concentration, worse short channel effect (SCE), and then lower V_{Tlin}. As for the V_{Tsat} at $V_{DS}=V_{DD}$=0.9V and DIBL=V_{Tlin}-V_{Tsat}, two more factors like finger-end fringing field and effective V_{DS} considering IR drop through parasitic resistances R_S and R_D should play an important role. As shown in Fig. 5(a), both MF and MR nMOS indicate smaller DIBL associated with the narrower W_F, which suggests the finger-end fringing field a dominant factor. As for the comparison between MF and MR nMOS, the finger-end fringing field from Raphael simulation, shown in Fig. 5(b) reveals the larger one achieved by MR nMOS and suggests the smaller DIBL, which can match the case of W_F=0.5μm but is against that of W_F=2 and 1μm. It means that the worse SCE due to lower boron concentration and higher effective V_{DS} due to smaller R_S may become two more dominant factors resulting worse DIBL in MR nMOS with W_F=2 and 1μm. Fig. 6(a) and (b) demonstrate promising results that MR nMOS can realize significant increase of I_{DS} and g_m through V_{GT} in comparison with MF nMOS. This improvement is considered originated from two major factors, such as higher μ_{eff} and smaller R_S.

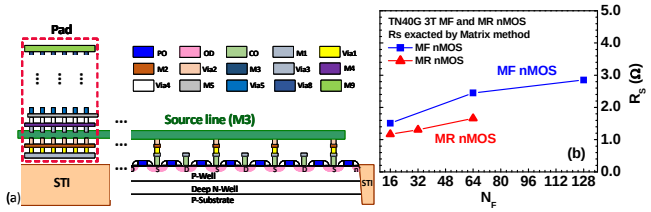

Fig. 3 (a) The cross section of MF device with the source line including contacts to S/D (b) R_S extracted by matrix method for MF and MR nMOS

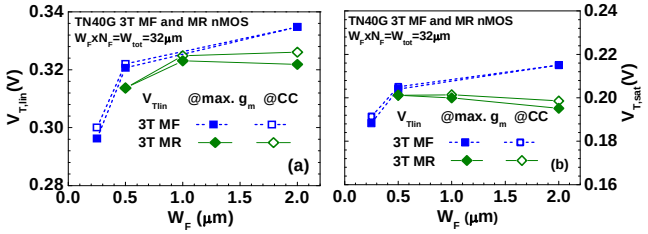

Fig. 4 Comparison of MF and MR nMOSFETs (a) linear region : V_{Tlin} vs. W_F at V_{DS} = 50 mV (b) saturation region : V_{Tsat} vs. W_F at V_{DS} = 0.9 V

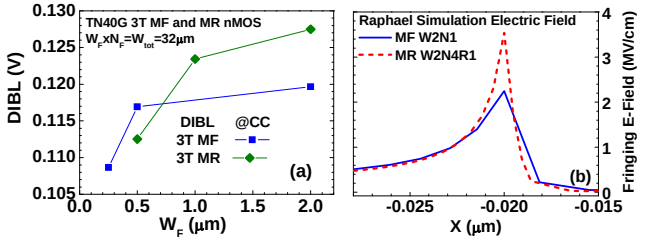

Fig. 5 Comparison of MF and MR nMOSFETs (a) DIBL versus W_F (b) finger-end fringing field along the channel direction and near the OD/STI corner region calculated by Raphael simulation.

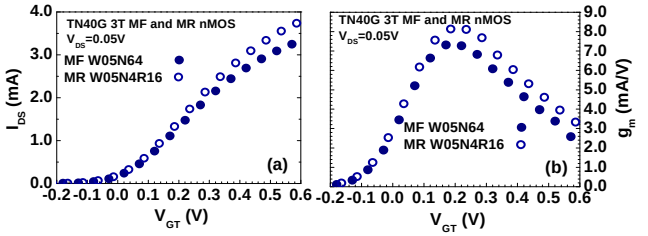

Fig. 6 Comparison of MF and MR nMOS : W05N64 and W05N4R16 (a) I_{DS} vs.V_{GT} (b) g_m vs. V_{GT} (V_{DS}=0.05V)

Table I provides a summary of basic device parameters extracted from MF and MR nMOS by using our proprietary extraction method [6]. The results show sub-35nm gate length, L_g =32.45nm/32.63nm and $T_{ox(inv)}$=19.501Å/19.502Å for MF/MR nMOS, i.e. very minor difference between two types of layout, but some significant difference in ΔW due to STI top corner rounding, such as 32.16nm and 50.32nm for MF and MR nMOS. This 1.56 times larger ΔW in MR nMOS can lead to the increase of $W_{eff}=(W_F+\Delta W)N_F$, which becomes another key parameter responsible for the increase of I_{DS} and g_m. Further investigation has been done by μ_{eff} extraction based on the linear I-V given by (1) with $I_{DS}(V_{GT})$ from measurement and key device parameters like L_g, $C_{ox(inv)}$, and W_{eff} as determined and summarized in Table I. As shown in Fig. 7 (a) and (b), the μ_{eff} vs. V_{GT} extracted from MF and MR nMOS indicate similar layout dependence, such as the lower μ_{eff} associated with the smaller W_F, which accounts for the impact from the increase of STI compressive $\sigma_{\perp}$. The comparison of MF and MR nMOS given by Fig. 7(c) indicates μ_{eff} enhancement realized by MR nMOS attributed to the smaller STI compressive $\sigma_{\perp}$. The final and most important verification has been made on high frequency parameters, such as $g_m=Re(Y_{21})$, $C_{gg}= Im(Y_{11})/\omega$, $C_{gd} = -Im(Y_{12})/\omega$, and f_T@model $=g_m/2\pi(C_{gg}-C_{gd})^{1/2}$ in saturation region as shown in Fig. 8 (a) ~ (d). First, the MR nMOS demonstrates the advantage of higher g_m through V_{GT} than MF nMOS, primarily due to lower R_S and larger W_{eff}. However, the MR nMOS reveals the penalty of larger C_{gg} owing to the increase of $C_{of}W_{eff}$ and $C_{f(poly\text{-}end)}N_F$ (Table 1) originated from separate source/drain for every gate finger and longer poly extension over STI. As a result, the increase of C_{gg} overwhelms that of g_m and leads to f_T degradation in MR nMOS compared to MF nMOS. As shown in Fig. 8(d). the MF nMOS can reach peak f_T up to 303~308GHz whereas the MR nMOS shows peak f_T around 280~289GHz. Thus, how to effectively reduce C_{gg} and keep higher g_m becomes the major challenge worthy of further research effort for high frequency performance improvement.

$$\mu_{eff} = \frac{I_{DS}}{\left(V_{DS} - I_{DS}\left(R_S + R_D\right)\right)} \frac{L_g}{C_{ox(inv)}\left(V_{GS} - V_T - \lambda V_{DS}\right)W_{eff}},\ 0 < \lambda < \frac{1}{2} \quad (1)$$

Table I Device parameters of the MF and MR nMOSFET

TN40G Parameters	Unit	MF nMOS	MR nMOS
L_g	μm	0.03245	0.03263
$T_{ox(inv)}$ (target)	A	19.5	19.5
$C_{of,sim}$	fF/μm	0.30517	0.29134
$C_{f(poly\text{-}end),sim}$	fF	0.03344	0.1187
$C_{ox(inv)}$	fF/μm^2	17.707	17.706
$T_{ox(inv)}=\varepsilon_0\varepsilon_{ox}/C_{ox(inv)}$	A	19.501	19.502
$\Delta W=(\alpha-C_{f(poly\text{-}end)})/(C_{ox(inv)}L_g)$	μm	0.03216	0.05032

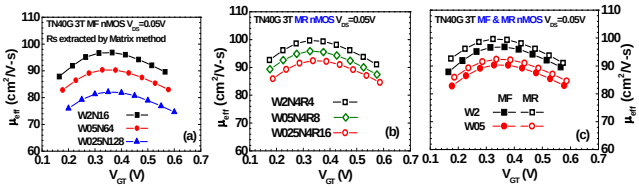

Fig. 7. μ_{eff} vs. V_{GT} extracted from linear I-V characteristics (a) MF nMOS (b) MR nMOS (c) comparison of MF and MR nMOS with various W_F and N_F

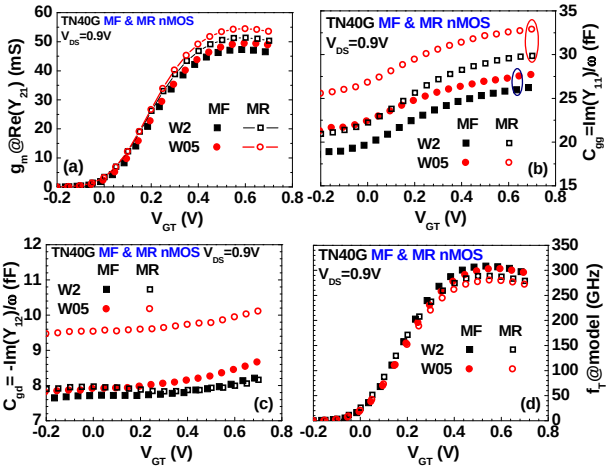

Fig.8 Comparison of MF and MR nMOS (a) g_m =Re(Y_{21}) (b) C_{gg} = Im(Y_{11})/ω (c) C_{gd} = -Im(Y_{12})/ω and (d) f_T @model =$g_m/2\pi(C_{gg}-C_{gd})^{1/2}$ vs. V_{GT} (V_{DS}=0.9V)

IV. Conclusion

MR nMOSFETs have been proven with the advantages of higher g_m due to μ_{eff} enhancement and R_S reduction compared to MF nMOSFETs. However, the undesired increase of C_{gg} originated from the 3-D fringing capacitances like C_{of} and $C_{f(poly\text{-}end)}$ overwhelms the g_m improvement and leads to the penalty of f_T degradation compared to the MF nMOSFETs. This in-depth analysis provides a useful guideline for layout optimization in RF and mm-wave devices design. Some more innovative layout solutions, aimed at higher g_m and lower C_{gg} for the ultimate goal of f_T boost to well above 300GHz become a new challenge worthy of further extensive research effort.

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