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Plasma Induced Damage on Inter-Metal Dielectric in Nano-meter FinFET Processes

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Abstract

In advanced CMOS FinFET technologies, tightly packed interconnect layers are expected to cause reliability concerns on inter metal dielectric (IMD) layers. In this study, two newly designed test patterns are used to investigate the plasma induced charging effect on the integrity of IMD films. Experimental data demonstrate that there are strong correlations between the plasma charging levels and damages found in IMD layers.

Introduction

Recently, in advanced back end of line (BEOL) processes, various plasma processes were introduced to ensure high aspect ratio structures and tightly packed interconnects are feasible[1]. These high-energy plasma processes are known to cause damages to transistors' gate dielectric stacks, therefore, many design rules limiting the size and length of interconnects are generated[2]. These may hinder the further scaling of design rules on BEOL layers. In addition, the introduction of low-k inter metal dielectric (IMD)[3] to avoid rising delays on these compact wiring structures can make the isolation films vulnerable to charging stresses during plasma processes [4]. More comprehensive studies of plasma charging damage (PID) on tightly packed interconnect structures are critical for setting new design rules and layout guidelines to ensure the reliability of the intricate circuit wirings implemented by advanced BEOL processes. With the support of the previously reported the novel in-situ PID recorders[5], differential test patterns are proposed and tested for early detections of the plasma charging damage on IMD films, enabling the investigation of the correlations between plasma charging level and the failure behaviors on the IMD structures.

New PID Test Structure for IMD Damage Detection

Plasma induced latent damages may occur within inter-metal dielectric layers between tightly packed interconnect patterns, as illustrated in **Fig. 1**. When design rules scales aggressively on BEOL layers, charges collected on the antennas may discharge through closely placed metal layers, Vias and/or contacts, causing stresses on IMDs. The in-situ PID recorders in **Fig. 2(a)** [5] are placed closely to the specific test patterns across a 12-inch wafer for establishing a reference plasma charging level. To study PID effects on IMD, two newly proposed differential test patterns for accentuate the latent damage caused by plasma induced stresses are introduced in **Fig. 2(b)** and **(c),** respectively. For type I samples, as a result of the rectifying effect of the n+/p-sub diode, PID stresses only occurs when electrons are collected on the antenna. On the other hand, type II samples experience stresses when the antennas are either positively or negatively charged. Samples are fabricated by a 16nm-standard FinFET/Cu BEOL process, where the same metal 3 antenna of 82000 μm^2 are attached. Differential structures are designed to screen out misalignment and process variation effects across samples.

Experimental Results and Discussion

In **Fig. 3**, the measured leakage current on patterns I and the reference PID levels from recorders on the same die show some similarity in distribution along the centerline of the 12-inch wafer. **Fig. 4** compares the IMD leakage current on measured on the left and right sides of a few examples. During plasma process, the weaker side is expected to become the main discharging path, hence, the V_{BD} from the side with early IMD breakdown is registered as the level correlated to PID stress. Using the V_{BD} obtained by this method, **fig. 5** compares the wafer maps of the PID level and V_{BD} from samples with both patterns. We found higher similarity between wafer maps of the V_{BD} from patterns and the reference PID levels. Distributions and correlations of V_{BD} obtained from type-I vs. type-II samples are compared in **Fig. 6(a)** and (b), respectively. Both plots suggests that type-II samples have a higher chance to exhibit a lower V_{BD}, which can be attributed to bi-directional stresses. **Fig. 7** summarized measured V_{BD} from the new test patterns vs. the reference PID levels on each die. Data indicate strong negative correlations between V_{BD} and plasma levels, namely, lower V_{BD} on samples experienced higher PID level. **Fig. 8** summarized the cumulative distributions of leakage current from left and right sides of both types of patterns. As the IMD thicknesses of 14nm are defined by the clearance between Metal 1 and Via1 masks, misalignments may cause systematic bias on the patterns. On average, I_{LL} is less than I_{LR} for type-I samples, while $I_{LL}<I_{LR}$ for type-II samples. The correlation between I_{LR} and I_{LL} in Fig. 9(a) reveals that process variations can affect leakage levels and prevents pure PID related readings. $R=I_{LR}/I_{LL}$ is found to be a better index for PID stress, where the distributions for both type of samples are plotted in Fig. 9(b). If the patterns are fully unbiased, the chances of the charging stress occurs on the right or left side should be equal. To correct for bias effect, R_N, normalized current ratio, is defined in **Fig. 10**. R_N from type-I samples correlate with PID readings, while R_N from samples subjects to bi-directional stress cannot be fully explained by the recorded PID levels.

Conclusions

New differential test patterns to study the effect of plasma induced charging on the integrity of IMD films is proposed and tested. Strong correlations between the plasma charging levels and damages found in IMD layers are established.

Acknowledgements

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References

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[3] Y.Y. Cheng, et al., in IITC, pp. 193-195, 1999.
[4] Y.P. Tsai, et al., in JEDS, pp. 875-883, 2018.
[5] C.H. Wu, et al., in IEDM, pp. 7.1.1-7.1.4., 2015.

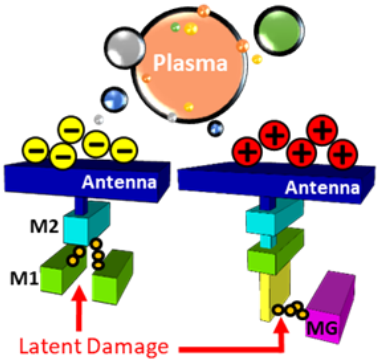

Fig. 1. Plasma induced latent damages occurs within inter-metal dielectric layers between tightly packed interconnect patterns.

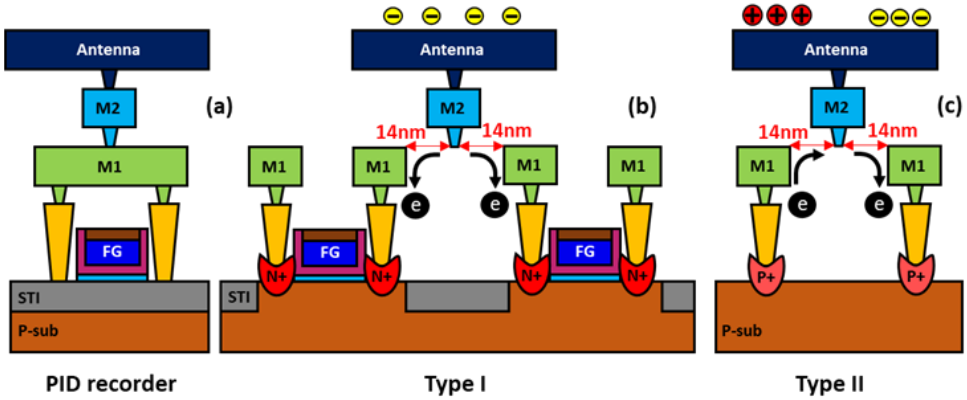

Fig. 2. 2D illustrations of (a) previously reported in-situ PID recorder, and newly proposed differential test patterns designed to accentuate the effect of latent damage caused by plasma induced (b) negative and, (c) bi-directional stresses.

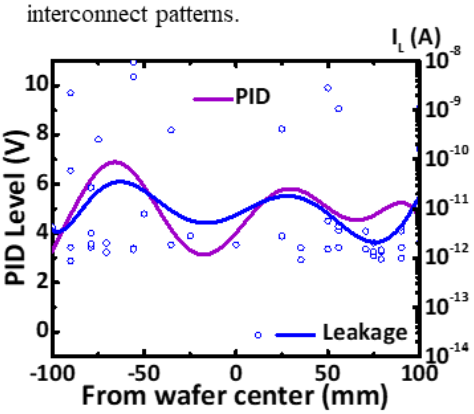

Fig. 3. Correlations between PID level from recorder and the leakage current @ 5V on samples of pattern I.

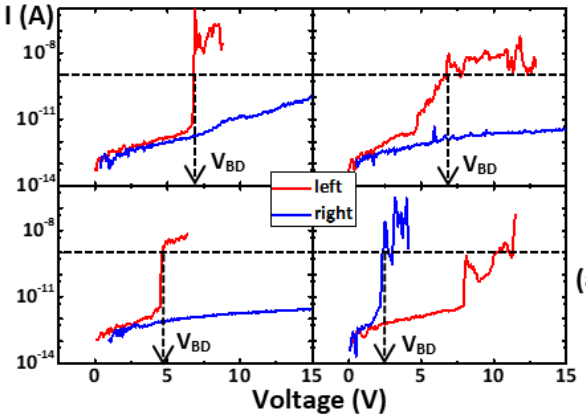

Fig. 4. IMD leakage current on differential test samples connected to antenna of 82000mm^2, V_{BD} is defined at the current level of 1nA.

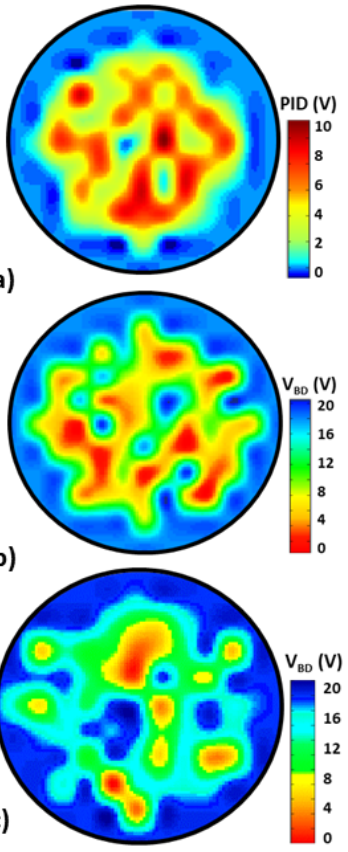

Fig. 5. Wafer maps of (a) the absolute value of PID voltage and that of the V_{BD} from (b) test pattern I and (c) test pattern II.

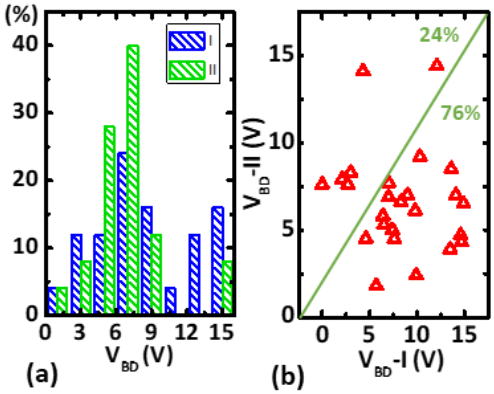

Fig. 6. Distributions (a) and correlations (b) of V_{BD} obtained from Pattern I and II.

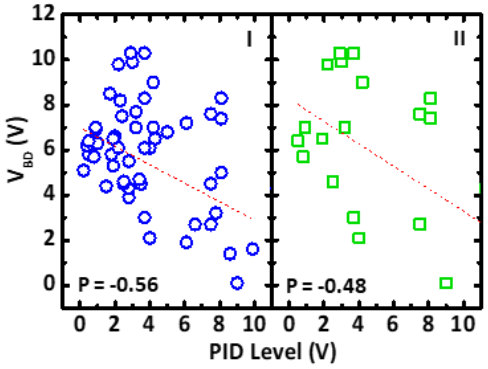

Fig. 7. Correlations between V_{BD} from Pattern I and II versus the PID levels.

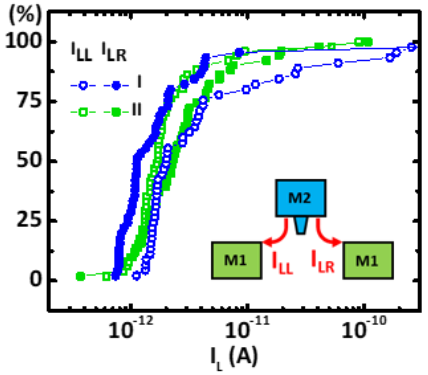

Fig. 8. Cumulative distributions of leakage current from left and right sides of Pattern I and II, compared.

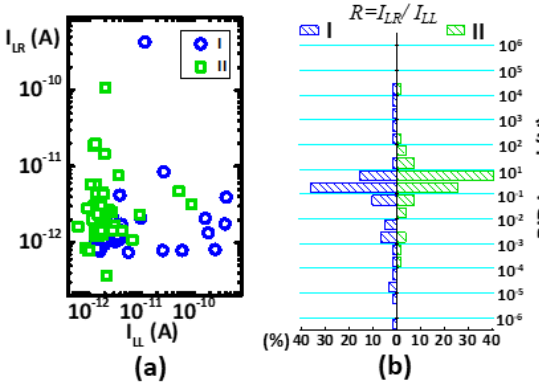

Fig. 9. (a) Correlation between leakage of the right to the left. (b) Distributions of current ratios of Pattern I and II.

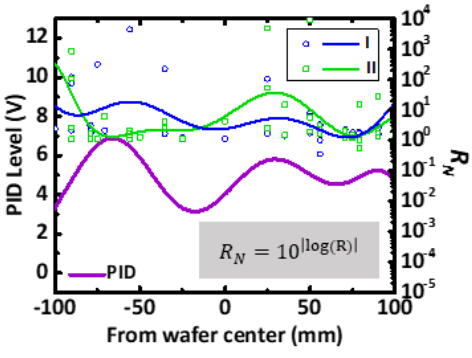

Fig. 10. Current ratio from both type I and II samples across wafer center as compared to PID levels.