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A New Structure of High-performance Source/drain Coupling Negative-capacitance FET Featuring Excellent Short-channel Controllability and Near Hysteresis-free

F. L. Li[1], E. R. Hsieh[2], C. H. Chiu[2], C. H. Liu[1], Steve S. Chung[2], T. P. Chen[3], S. A. Huang[3], T. J. Chen[3], and Osbert Cheng[3]
[1]*National Taiwan Normal University, Taiwan* [2]*Department of Electronics Engineering, National Chiao Tung University, Taiwan*
[3]*United Microelectronics Corporation (UMC), Taiwan*

Abstract

In this work, we proposed a new structure of Negative-capacitance (NC) FET by using an NC S/D-to-gate coupling scheme. With benefits of this scheme, the severe remote scattering induced from the dipoles in HZO layer will be effectively alleviated so as to enhance the performance with higher I_{on}, much lower S.S., better short-channel controllability, and even near hysteresis-free, in comparison to those of the conventional NC-gate-coupling scheme. In order to design an optimized NC-S/D-coupling FET, an equivalent circuit was also developed to calculate NC values. Results have shown that the NC effects are proportional to the area of HZO dielectric between S/D and gate. Finally, the design guidelines of high-performance and excellent short-channel-controllability for NC S/D-coupling FET will be provided.

1. Introduction

To realize IoT, ultra-low power transistors are a prerequisite. Negative capacitance field effect transistor (NCFET) has come into place because of their potential for achieving steeper subthreshold swing, S.S., (< 60mV/decade) and larger on-current (I_{on}) [1-2]. As far as high-performance NCFET is concerned, it is important not only to match the capacitance of ferroelectric HZO MIM with the gate-dielectric of n-FET but also to consider how the remote scattering events of the flip-flop dipoles in HZO layer affect the effective mobility in the channel when the HZO layer is made on the gate as NCFET. As is well known, although the overall gate capacitance of NC-gated FET can be greatly enhanced through NC effect, it does not guarantee the enhancement of the drain current (I_{on}) due to the serious mobility degradation [3,4]. In this work, we will propose a new structure of NC-S/D-coupling FET, Fig. 1, where the HZO layer is not directly connected to the gate but connected between the gate and S/D. By doing so, the NC effect can not only still be coupled to the gate capacitance, but the remote scattering from the HZO dipoles can be avoided. Furthermore, from the equivalent circuit concept, the extraction method of NC values has been developed. Finally, both theoretical and experimental results of NC-S/D-coupling FETs exhibit higher Ion, smaller S.S., smaller DIBL, and even hysteresis-free characteristics.

2. Device Preparation

The ferroelectric layer composed of HZO (5nm) is sandwiched by TiN top/bottom electrode and prepared in post metal annealing temperature of 550^0C. HZO MIM were respectively connected in parallel (Fig. 1) and in series (Fig. 2) with the 28 nm-n channel FET, with different device dimensions.

3. Results and Discussion

A. A New S/D Coupling NC-FET – At first, we examine the difference between the new structure of NC-S/D-coupling FET and the conventional NC-gate-coupling FET. Fig. 1 is the schematic of NC-S/D-coupling FET, where we connected the HZO MIM in parallel between the gate and drain (drain coupling) or the gate and source (source-coupling) of the n-FET, respectively. Fig. 2 is the schematic of *conventional* NC-gate-coupling FET, where HZO MIM is made directly on the top of FET gate. Meanwhile, this new S/D-coupling one couples the NC effect to the gate so as to enhance I_d and is expected to alleviate the remote scattering in the channel.

B. Mobility Degradation in Gate Coupling- When V_{gs} applied, HZO will modulate the channel carriers. Our experimental data shows that maximum value of effective mobility has been degraded dramatically in the gate-coupling one, Fig. 3, although the overall gate capacitance can be enlarged via the NC effect. The reason of effective mobility degradation is that remote scattering events due to the HZO dipoles will seriously fluctuate the HZO dipoles and disturb the transporting carriers in the channel and then increase the phonon scattering events thereby (Fig. 4), which will seriously degrade the mobility, leading to a reduction of the I_{on}. In Fig. 5, I_dV_{gs} of the conventional gate coupling one shows not only a lower I_{on} but also those non-improved I_{off}, S.S., and hysteresis, which is because of not well-matched capacitance between the HZO and gate oxide and more importantly, deterioration of the effective mobility [3].

C. Enhanced I_{on} and SS in Source/Drain Coupling

Therefore, in order to reduce the remote scattering events caused by HZO dipoles, a new structure of NC-S/D-coupling FET has been developed. In Fig. 6, the I_dV_{gs} of the drain-coupling one shows an enhanced I_{on}. Moreover, a lower I_{off}, steeper S.S. and reduced hysteresis are also obtained, compared to those of the control nMOSFET and gate coupling one. Fig. 7 is the comparison of I_dV_{ds} for S/D coupling ones with the control and gate coupling one exhibits larger G_d in the triode region of I_dV_{ds}, which indicates a higher effective mobility. Furthermore, an enhanced I_d in the saturation region (V_{ds} = 1V) for the S/D coupling ones are also observed. In order to explain how the HZO capacitance couples to the gate capacitance, the equivalent circuit of drain-coupling has been derived. It is noticed that the source-coupling one can be explained in a similar way because of the S/D symmetric construction of a MOSFET. The *left* of Fig. 8 is the equivalent circuit model of the drain coupling one and can be simplified on the *right* of Fig. 8. To make sure the existence of NC effect, the term $_s/V_{gs}$, should be greater than unity, and thus the circuit on the *right* of Fig. 8 can be expressed by Eq. (1) in Table 1. Once the $_s/V_{gs}$ is greater than a unit, the amplification of the internal voltage between HZO MIM and nMOSFETs can be confirmed, i.e., existence of NC effect. Moreover, C_{DIBL}, C_{ox} and C_{dep} can be extracted in Table 1 as well. Based on these parameters and the simplified circuit on the left of Fig. 8, Fig. 9 shows that S/D coupling capacitance from HZO to the gate oxide, $|C_{FE}|$, is proportional to the area of HZO dielectric between S/D and gate. Fig. 10 are the experimental results. It was found that the I_{on} enhancement is proportional to the channel width as the width is longer than 2 μm, which ensures the correctness of our theory. Furthermore, the experimental results of S/D-coupling ones in Fig. 10 also show the reduction of the remote scattering when the width is smaller than 2 μm. Fig. 11 shows the enhanced I_{on}, which is attributed to an enhanced drain conductance (g_d). Also, NC-S/D-coupling FET shows 65% boost of g_m (Fig. 12).

D. Short Channel Effect of Source/Drain Coupling

As far as the short channel controllability is concerned, the hysteresis of S/D coupling one at different V_{ds} biases is greatly reduced and even to be near hysteresis-free characteristics, compared to that of the gate-coupling (Fig. 13). In addition, S/D-coupling also shows lower V_{th} and smaller DIBL with increasing V_{ds} (Fig. 14). Thanks to well-controlled DIBL, the averaged subthreshold swing of S/D-coupling one will not increase as the V_{gs} or V_{ds} ramps and keeps as low as the values near or even below 60mV/dec. (Fig. 15&16). As a result, NC-S/D-coupling FET not only shows an excellent short-channel controllability but also the reduction of hysteresis, nearly approaches to zero.

In summary, we have developed a new structure of NC-S/D coupling FET successfully, the summaries of silent features are given in Table 2. NC-S/D-coupling FETs have shown their potential in achieving high performance and low power transistor with enhanced Ion and much better short-channel controllability. Inherent mobility degradation issue in conventional architecture (gate-coupling one) has been solved by alleviating the remote scattering events with S/D coupling scheme so that a higher I_{on} and steeper subthreshold swing can be achieved. In terms of short channel effect, DIBL and SS_{avg} with increase of V_{ds} have been significantly improved in S/D coupling scheme, and more importantly, the near hysteresis-free can be also obtained. Finally, the radar chart of Fig. 18 shows S/D-coupling scheme exhibits superior performance in general, with reference to the conventional architecture, providing a promising solution for NC-FET design.

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References: [1] S. Salahuddin et.al., ***Nano Lett.***, 2008. [2] E. Ko, et al., ***IEEE EDL***, p. 418, 2017. [3] Y. C. Luo, et al., ***VLSI-TSA***, p. 102, 2019. [4] Y. C. Luo, et al., ***SSDM***, p. 189, 2018.

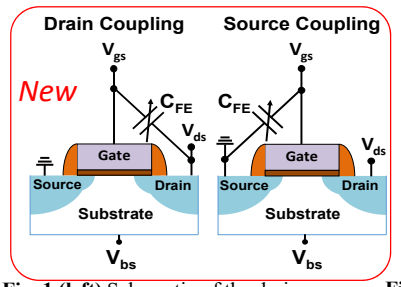


Fig. 1 (left) Schematic of the drain coupling and **(right)** source coupling ***NC-FET.*** A 5-nm thick HZO film is connected in parallel with nMOSFET.

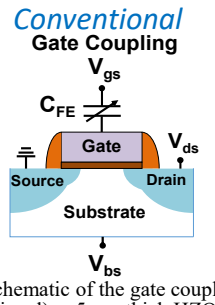


Fig. 2 Schematic of the gate coupling (conventional): a 5-nm thick HZO film is connected to the gate of an nMOSFET.

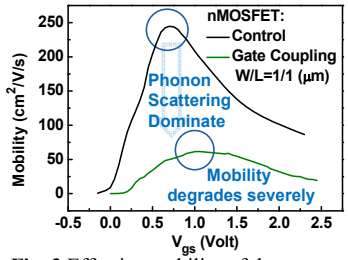


Fig. 3 Effective mobility of the gate coupling and nMOSFET with W/L = 1/1 μm: the peak mobility has been degraded severely, as a result of phonon scattering event.

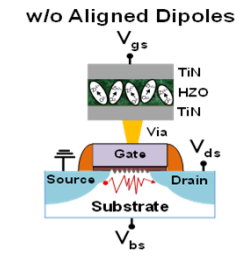


Fig. 4 HZO dipole fluctuation of the gate causes the remote scattering event in the channel which induces the phonon scattering, thus reduces the effective mobility.

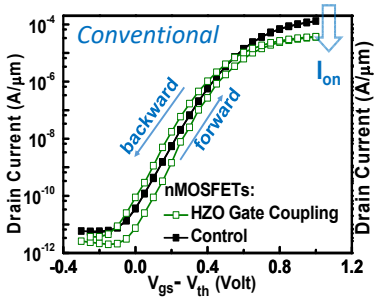


Fig. 5 $I_d V_{gs}$ of NC-FET with gate coupling, shown in Fig. 2, with HZO MIM area of 100×100 μm². The gate coupling shows degraded I_{on} and comparable S.S., compared with the nMOSFET.

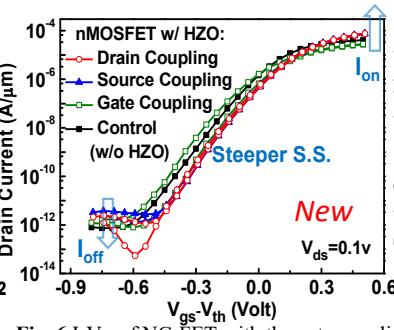


Fig. 6 $I_d V_{gs}$ of NC-FET with the gate coupling, source coupling, and drain coupling. The drain coupling one shows an enhanced I_{on}, lower I_{off}, reduced hysteresis, and an improved subthreshold swing, compared to those of the original nMOSFET and the gate coupling one.

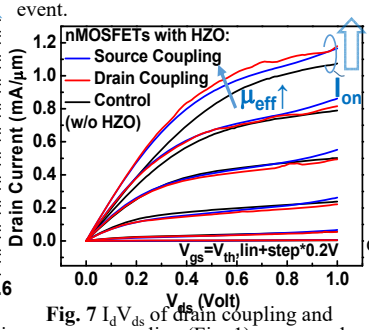


Fig. 7 $I_d V_{ds}$ of drain coupling and source coupling (Fig. 1), compared with that of the nMOSFET. The drain coupling shows larger effective mobility and an enhanced I_{on} in saturation region compared to the original nMOSFET.

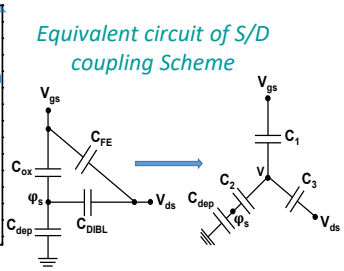


Fig. 8 Equivalent circuit model of drain coupling. The C_{FE} (capacitance of HZO MIM) is in parallel with $C_{ox,MOS}$ (gate capacitance of nMOSFET).

$$\frac{\partial\varphi_S}{\partial V_{gs}} = \frac{C_1}{C_{1+}C_{3+}\frac{C_{dep}(C_{1+}C_{2+}C_3)}{C_2}} \quad (1)$$

$$C_1 = \frac{1}{C_{ox+}C_{FE+}\frac{C_{ox}C_{FE}}{C_{DIBL}}} \quad (2)$$

$$C_2 = \frac{1}{C_{ox+}C_{DIBL+}\frac{C_{ox}C_{DIBL}}{C_{FE}}} \quad (3)$$

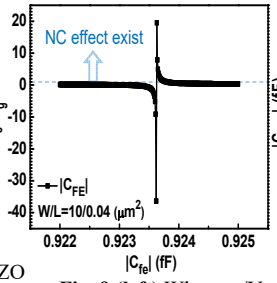
$$C_3 = \frac{1}{C_{DIBL+}C_{FE+}\frac{C_{DIBL}C_{FE}}{C_{ox}}} \quad (4)$$

$$C_{DIBL} = \frac{(V_{t,long} - V_{t,short})C_{ox}}{V_{ds}} \quad (5)$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (6)$$

$$C_{dep} = \frac{\varepsilon_{si}}{W_{dep}} \quad (7)$$

Table 1 To calculate the value of C_{FE} (capacitance of HZO MIM) in drain coupling, the circuit (Fig. 8) can be expressed by Eq. (1). C_{DIBL}, C_{ox}, and C_{dep} can be calculated from (5)~(7), then are substituted into (2)~(4) to get C_1, C_2 and C_3. The C_{FE} value, Eq. (1) can be finally determined.



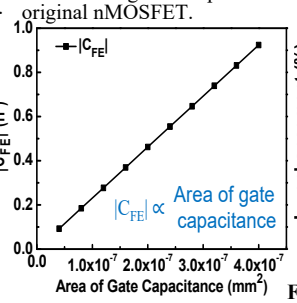


Fig. 9 (left) When $\psi_s/Vg > 1$, NC effect exists. The value of |CFE| is calculated from Table 1. **(right)** The |CFE| value in different gate-capacitance areas. |CFE| is directly proportional to the area of gate capacitance.

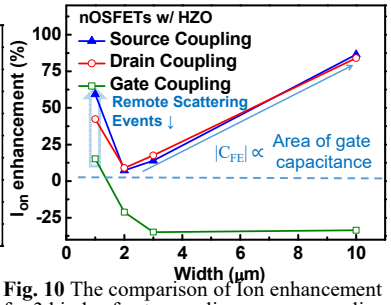


Fig. 10 The comparison of Ion enhancement for 3 kinds of gate coupling, source coupling, and drain coupling. The drain and source couplings did not have remote scattering effect such that Ion can be largely improved.

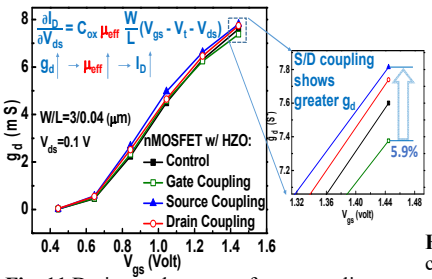


Fig. 11 Drain conductance of gate coupling, source coupling, and drain coupling, compared with that of the original nMOSFET. The source coupling one show an enhanced g_d with 5.9%.

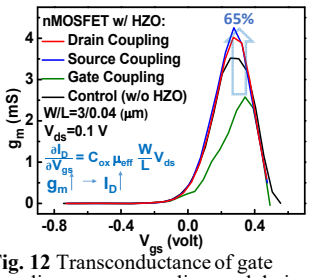


Fig. 12 Transconductance of gate coupling, source coupling, and drain coupling in comparison to that of the original nMOSFET. The drain and source coupling shows an enhanced g_m with 65%.

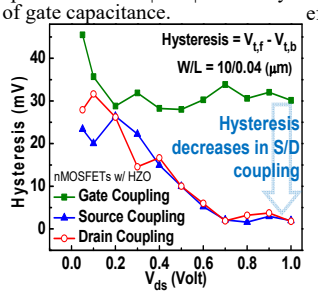


Fig. 13 Hysteresis of gate coupling, source coupling, and drain coupling. The drain coupling and source coupling shows a decreased hysteresis in DC analysis.

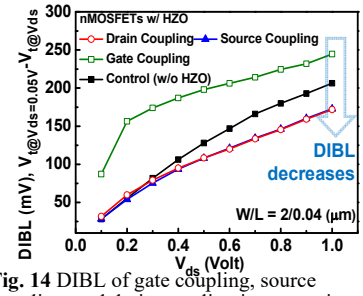


Fig. 14 DIBL of gate coupling, source coupling, and drain coupling in comparison to that of the original nMOSFET. The drain coupling and source coupling shows an improved DIBL in short channel effect.

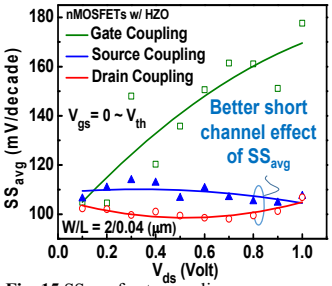


Fig. 15 SS_{avg} of gate coupling, source coupling, and drain coupling. The drain coupling and source coupling show much better short channel effect of SS_{avg}.

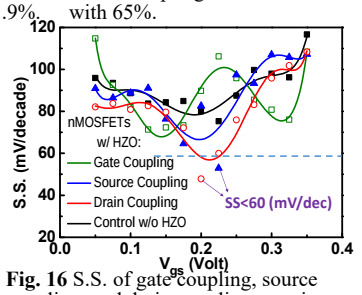


Fig. 16 S.S. of gate coupling, source coupling, and drain coupling ones in comparison to that of the original n-FET. Drain and source couplings show an improved S.S. and the minimum value of S.S. is smaller than 60 mV/dec.

	Gate Coupling	Source Coupling	Drain Coupling
I_{on} Enhancement (V_{ds} = 1V)	-35%	38%	40%
$SS_{minimum}$ decrease (60mV/dec - $SS_{minimum}$)	-11.33	7.05	12.17
g_d (V_{ds} = 0.1V)	-2.9%	2.8%	1.8%
g_m (V_{ds} = 0.1V)	-26.8%	20.9%	14.3%
DIBL decrease (V_{ds} = 1V)	-18.5%	16.2%	16.7%

Table 2 Comparison of the gate coupling, source coupling, and drain coupling with W/L=2/0.04 (μm)

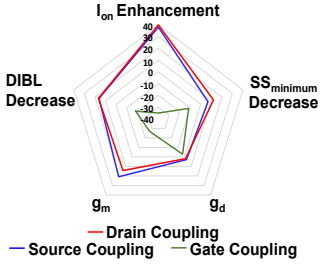


Fig. 17 Comparisons of radar chart for the gate coupling, source coupling, and drain coupling. S/D couplings show better performance.