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Synthesis and Characterization of Topological Crystalline Insulator SnTe Nanowires

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Abstract

Surface orientation dependent topological surface states have been found in topological crystalline insulator SnTe. Study on specific topological surface states demands more understanding of the formation mechanism of SnTe facets. Here, we report on the synthesis and characterization of SnTe nanowires with different morphology. The heating process of chemical vapor deposition (CVD) is divided into two steps, and a sudden increase of substrate temperature is introduced between two steps. Straight and kinked nanowires are obtained by this technique under different conditions. High resolution transmission electron microscopy observation shows {100} surfaces in both straight and kinked nanowires. This result suggests that the minimum of surface energy for SnTe crystal growth is influenced by more factor than the substrate temperature. Electrical properties of SnTe nanowires are investigated. Weak antilocalization is detected in SnTe nanowire at low-temperature by magnetotransport measurement.

1. Introduction

Topological crystalline insulators (TCIs) are new states of matter with nontrivial topological electronic structures produced by crystal symmetries. SnTe is one kind of TCI material with point-group symmetry protected surface states. Detailed theoretical calculations and experimental measurements reveal that the surface states of SnTe crystal are facet-dependent on (100), (110), (111) surfaces [1]. Great efforts are made to understand the formation mechanism of outer surface of SnTe crystal in order to prepare and study SnTe crystal with specific facets.

Chemical vapor deposition (CVD) is a simple method to synthesize SnTe nanostructures with different outer facets. CVD experiment results reveal that the surface orientation of SnTe nanostructures should be controlled by a balance between the minimum of surface energy and the substrate temperature, which decides the stoichiometry of Te and Sn. A model describing the morphology of SnTe nanostructures has been proposed based on the substrate temperature dependent surface energy, which explains more appearance of {111} facets than {100} facets [2].

Kinking represents a variation of the nanowire's axial orientation induced by a sudden change of growth parameters. Analysis of the structure of kinked nanowire reveals the energy required for crystal stacking in a new direction. We change the substrate temperature during the growth period of SnTe nanowires in CVD experiment. All kinked SnTe nanowires synthesized by this way show growth axis transition from <020> to <200>. The appearance of same {100} outer facets before and after the kinking indicates some decisive factor other than the substrate temperature. We also investigate the transport property of thin SnTe nanowires. The result of magnetotransport measurement reveals strong spin-orbit coupling in SnTe nanowires.

2. Results and discussion

Method

The growth of SnTe nanowires is carried out with a home-made CVD system. A tube furnace is mounted on two parallel rails and can move freely within a very short time. SnTe powder (purity 99.999%, Xintai Co.) is used as the source for nanowire growth. SiO_2(300 nm)/Si plates covered with 3 nm gold film are used as the substrate. The heating temperature of the furnace is set in a range of 600-700°C. The heating time is 30 min. In some experiments, after heating 15 minutes, the furnace is moved ~ 1 cm. This small movement creates a steep increase of the substrate temperature (~ 80°C) in the latter 15 min heating period.

Four-terminal devices are fabricated to investigate electrical characteristics of SnTe nanowires synthesized in this work. The SnTe nanowires are mechanically transferred from growth substrates onto a 200-nm-thick SiO_2/Si substrate with predefined positioning markets for device fabrication. The SnTe nanowires with diameter of 70 – 120 nm are selected to define electrical contacts by electron beam lithography (EBL) process. Then a deposition of 100 nm Cr using sputter can ensure a conformal deposition of metal electrodes on the SnTe nanowires. The electrical and magnetic measurements are carried out in a physical property measurement system (PPMS) cryostat using a standard lock-in technique.

Characterization

The morphology of nanowires grown with stable and two-step substrate temperature is shown in Fig. 1a and 1b, respectively. Thick and straight nanowires are observed on the substrate heated at 700°C stably. Most nanowires have a diameter larger than 200 nm and a length of more than 10 μm. Instead of nanostructures with inclining {111} facets, kinked nanowires with perpendicular {100} surfaces are

found in some samples prepared after the furnace movement (shown in Fig. 1b).

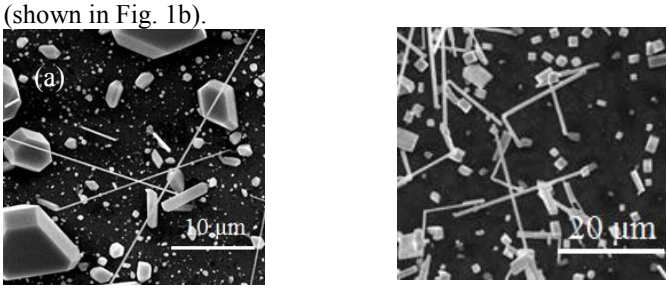

Fig. 1 SEM image of (a) straight SnTe nanowires grown with stable substrate temperature (700°C), (b) kinked nanowires grown with two-step substrate temperature.

We investigate the structure of kinked nanowires by HRTEM detailedly. Figure 2a shows a TEM image of the corner part of a kinked SnTe nanowire. Right angle is measured in this kinked nanowire. Single crystalline structure of SnTe is observed and no defect is found in both sides. SAED pattern of three points in this kinked nanowire are shown in Fig. 2b - 2d. Neither {111} facet nor defect is found in kinked nanowire. Based on HRTEM image and SAED pattern, {100} facets of SnTe are confirmed in both sides of kinking, which corresponds to nanowire growth before and after the sudden change of the substrate temperature. This fact indicates that the tendency of SnTe growth with {100} surfaces is rather strong even in a temperature-changing environment.

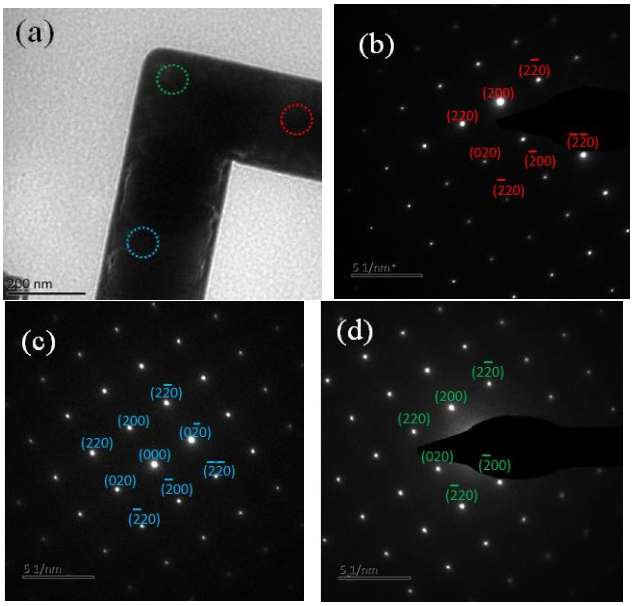

Fig. 2 (a) TEM image of a kinked SnTe nanowire, (b), (c), and (d) SAED pattern of corresponding point in (a).

Device

Thin and straight SnTe nanowires grown at 600°C with moving the furnace are used to fabricate four terminal devices. Figure 3a shows the SEM image of a measured device. The inset of Fig. 3a shows AFM scanning plot of the measured nanowire. The resistance R decreases monotonically with the reduction of temperature. Most SnTe nanowires measured in this work show similar resistance reduction at low temperature. Such metallic transport is a typical conduction behavior of SnTe nanostructures, probably due to a common structural defect in SnTe, high density of Sn vacancy. The measured magnetoconductance ΔG is shown in Fig. 3b. The upward cusp near zero magnetic field suggests the weak antilocation (WAL) effect that originates from strong spin-orbit coupling in SnTe nanowires.

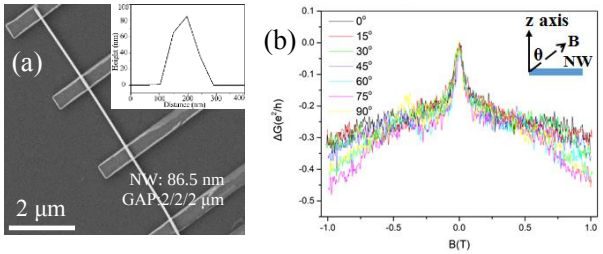

Fig. 3 (a) SEM image of measured four-terminal device, Inset: AFM scanning plot of the nanowire. (b) Magnetoconductance measurement at 2K.

3. Conclusions

In summary, we demonstrate the growth of SnTe nanowires by two-step substrate temperature technique. Smooth {100} surfaces are observed in the kinked SnTe nanowires grown at 700°C after the movement of furnace. Weak antilocalization is detected in single SnTe nanowire at low-temperature by magnetotransport measurement.

Acknowledgements

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References

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