Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp633-634

Characteristic Variability and Random Telegraph Noise of Gate-All-Around Silicon Nanowire MOSFETs with Asymmetric Dual Spacer Induced by Single Charge Trap

Sekhar Reddy Kola[1,2], Yiming Li[1-5,*], Narasimhulu Thoti[1,2], Chieh-Yang Chen[1,3], and Wen-Li Sung[1,3]

[1]Parallel and Scientific Computing Laboratory; [2]EECS International Graduate Program, [3]Institute of Communications Engineering; [4]Department of Electrical and Computer Engineering; and Center for mmWave Radar System and Technologies, National Chiao Tung University, 1001 Ta-Hsueh Rd., Hsinchu 300, Taiwan; *Tel: +886-3-5712121 ext. 52974; Fax: +886-3-5726639; Email: ymli@faculty.nctu.edu.tw

Abstract

We study effects of asymmetric dual spacer (ADS) with various spacer materials on characteristic fluctuation of gate-all-around (GAA) silicon nanowire (NW) metal oxide semiconductor (MOS) field effect transistor (FETs). Based on experimentally validated device simulation, the results show that the DC variation is marginal, but the AC variation is significant owing to influence of low-κ spacer on parasitic capacitance. Compared with the device without spacer, the device with ADS possesses 68.8% off-current decrement and 29.4% on-current increment. The gate and fringing capacitances of the device with ADS is much reduced, compared with those with HfO_2 spacer. We do further compare the random telegraph noise (RTN) induced by acceptor-type single charge trap (SCT) for sub-7-nm technological nodes. The signal of RTN ($\Delta I_D/I_D \times 100\%$) purely depends on area, position and density of interface trap (D_{it}) of the SCT along the channel interface. The signal of RTN for the trapping and de-trapping of the device with and without spacer is about 2.3%.

1. Introduction

GAA Si NW MOSFET devices are the ultimate structures in the fabrication of VLSI chips. Scaled devices will continuously benefit IC technologies, but it suffers from more severe short-channel effects (SCE). In the meanwhile, the ultra-small device face various fluctuations induced by, such as random dopant fluctuation (RDF), work function fluctuation (WKF), process variation effects (PVE) and line edge roughness (LER) [1-2]. For example, GAA Si NW MOSFET devices for sub-5-nm technology nodes, have encountered various fluctuation problems [3-6]. Devices with various spacers can improve device performance and suppress SCE [7-8]; and the superior gate control was investigated [4-5]. Unfortunately, the RTN induced by SCT for cylindrical-shape-channel GAA Si NW MOSFET has not been clearly investigated yet. In this work, we study DC/AC characteristics of the explored N-type devices with different spacer materials including low-κ (SiO_2), high-κ (HfO_2), Si_3N_4, and asymmetric dual spacer (ADS; 50% SiO_2 + 50% HFO_2) [7-8]. The RTN induced by the acceptor-type SCT at the middle of interface of Si/SiO_2 is further investigated and discussed.

2. Device Simulation Methodology

The device simulation is performed intensively by solving a 3D quantum-mechanically corrected density-gradient drift-diffusion (DG DD) transport model that has been validated through the nonequilibrium Green's function (NEGF) results by tuning the electron effective mass [6]. To provide the best accuracy of simulation, not shown here, we also calibrated with our simulation with measured GAA Si NW devices [6], where the band-to-band tunneling from source to drain is considered [9]. The simulated device has cylindrical-shape channel with an effective 10-nm-gate length is considered featuring for sub-5-nm nodes. Figs. 1(a)-(b) show the adopted device with ADS and its cross-sectionals view along the channel is inferred. For the ADS we cover SiO_2 and HfO_2, as shown in Fig. 1(a), to envelop S/D extension [7-8]. The device dimensions and the achieved SCE parameters of the nominal device are listed in Tab. I. The 3D SCT has also cylindrical type with 2 nm length and 0.6 nm radius in the interface of Si/SiO_2 [10]. The explored device has the most severe impact of SCT on RTN, from low to high density of interface trap (D_{it}). For all the devices the location of SCT is considered at middle of the channel.

3. Results and Discussion

As depicted in Fig. 1(c), the 21% improvement of on-state and 35.8% decrement of off-state normalized currents for the device ADS, compared with the case of low-κ spacer are achieved. Figs. 2(a) and (b) show the I_D-V_G characteristics considering the impact of spacers on the enhancement of on-state current and reduction of the off-state current, the extracted values are listed in Tab. II. The analysis is made having low-κ, Si_3N_4, high-κ and ADS spacers at linear and saturation conditions. For the device with ADS, the normalized on-current increases (about 29.48% and 27.8% increases) for both the linear and saturation conditions, respectively. Similarly, 30.5% and 68.86% reductions are observed for the normalized off-current. At high gate bias, the fringing electric field would penetrate from the S/D extensions regions owing to heavy dopant; thus, the gate fringe field cannot change the resistance of S/D extensions. This leads to relatively higher on-current and lower off-currents for devices with ADS and high-κ spacer. From Fig. 2(c), it is noticed that gate to drain capacitance increases with the increase of gate voltage. Particularly, for high dielectric spacer large gate to drain capacitance has been observed.

The amount of gate capacitance is increased heavily with the high-κ spacer due to its high parasitic capacitance. Thus, it affects the fringe capacitance in S/D extensions and the fringe capacitance increases when the spacer permittivity increases. Very extensive normalized gate capacitance varying from 32% to 65% has been observed for the device varying from low-κ to high-κ, but for the ADS spacer has 48%, as shown in Fig. 3(a). The explored GAA Si NW MOSFET has suppressed gate capacitance with increased S/D extensions is shown in Fig. 3(b). For the case of DC, increased the S/D extensions, the I_D-V_G also decreases, respectively, as shown in Fig. 3(c). Fig. 4(a) indicates the normalized gate capacitance as higher (about 60% deviation) for the device with a high-κ spacer due to the effect of extensions permittivity and parasitic capacitance. But the device with ADS has lies in between low-κ and high-κ. Figs. 4(b) and (c) show the signal of RTN induced by SCT, due to low conduction carriers at low gate voltage, the RTN is increased with increased D_{it} of acceptor-like traps. Thus, the device with spacer has very low leakage current; the largest one is only 2.39%, as shown in Fig. 4(c) for nominal cases.

4. Conclusions

In summary, the ADS spacer has wonderful characteristics compared to other spacer materials; in particular, for the off-current it is about 68.8% reduction and the boost of on-current is up to 29.4%, compared with the device without spacer. The signal of RTN induced by SCT does not be altered significantly for the explored GAA Si NW MOSFETs with and without ADS.

Acknowledgment

This work was supported in part by the Ministry of Science and Technology, Taiwan, under Grant MOST 106-2221-E-009-149, Grant MOST 106-2622-8-009-013-TM, Grant MOST 107-2622-8-009-011-TM, Grant MOST 107-2221-E-009-094, and Grant MOST 107-3017-F-009-001, in part by the "Center for mmWave Smart Radar Systems and Technologies" under the Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the Ministry of Education in Taiwan.

References

[1] Y. Li, et al., *Int. J. Nanotech.*, pp. 1029-1038, 2014.
[2] Y. Li, et al., *IEEE T. SM*, pp. 509-516, 2010.
[3] Y. Li, et al., in *IEDM Tech. Dig.*, pp. 887-890, 2015.
[4] M. L. Fan, et al., *IEEE T ED*. **59**, pp. 2227-2234, 2012.
[5] Y. Li et al., *IEEE Trans. Nano. Tech.,* **4**, pp. 510-516, 2005.
[6] W.-L. Sung, et al., *IEEE T. ED*, **65**, pp. 2638-2646, 2018.
[7] A. B. Sachid, et al., *IEEE T ED*. **64**, pp. 5181-5187, 2017.
[8] A. B. Sachid, et al., *IEEE T ED*. **64**, pp. 1861-1864, 2017.
[9] Schenk et al., *SSE*. **36**, PP. 19-34, 1993.
[10] S.-C. Hsu and Y. Li, *Nanoscale Res. Lett*., **9**, pp.633, 2014.

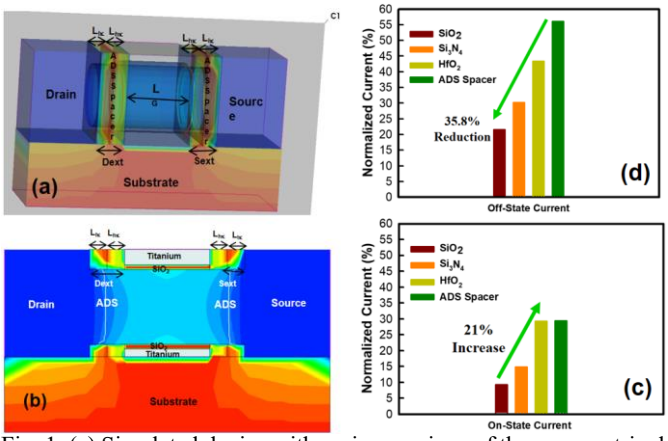

Table I List of the N-type nominal device parameters, the achieved DC characteristic, and the SCE parameters. The gate length of 10 nm follows ITRS projection for sub-5-nm technological nodes.

Parameter	Value
Gate Length (L_G) (nm)	10
Channel Doping (cm^{-3})	$5e^{17}$
S/Dext Length (nm)	5
S/D Doping (cm^{-3})	$1e^{20}$
S/Dext Doping (cm^{-3})	$4.8e^{18}$
EOT (nm)	0.6
I_{ON} (A)	$7.634e^{-6}$
I_{OFF} (A)	$1.596e^{-11}$
I_{ON}/I_{OFF} Ratio (A/A)	$4.798e^{5}$
SS (mV/dec)	72
DIBL (mV/V)	65

Table II List of the normalized (%) on- and off- state currents for the explored device with different spacers. The calculation is with respect to the device without spacer at $V_D = 0.05$ V and $V_G = 0.6$ V. Notably, the GAA Si NW MOSFETs with ADS covered by 50% SiO_2 and 50% HfO_2 exhibit very promising performance boost among all cases.

Parameter	SiO_2	Si_3N_4	HfO_2	ADS
On-State Current (increase)	9.3	14.9	29.3	29.5
Off-State Current (decrease)	21.6	30.3	43.41	56.1

Fig. 1. (a) Simulated device with various regions of the asymmetric dual spacer (ADS) device. (b) A cross-sectional view along the channel of cut (c1) from plot (a). (c) The normalized on-state current ($V_G = 0.6$ V and $V_D = 0.05$ V) with respect to the device without spacer. (d) The normalized off-state current ($V_G = 0.0$ V and $V_D = 0.05$ V) with respect to the device without spacer. Notably, compared with the results of device with SiO_2 spacer (brown), the case of ADS (green) has 35% off-state current reduction and 21% on-state current increase.

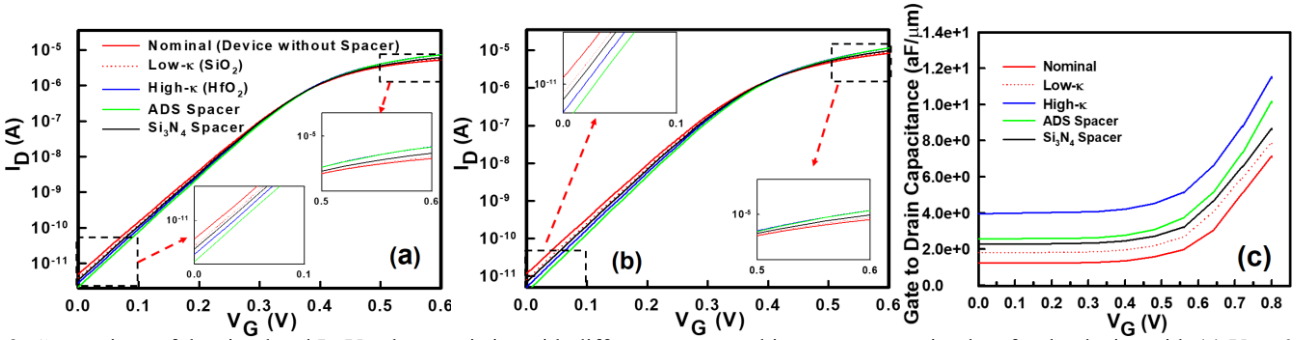

Fig. 2. Comparison of the simulated I_D-V_G characteristics with different spacer and insets are zoom-in plots for the device with (a) $V_D = 0.05$ V and $V_G = 0.6$ V and (b) $V_D = V_G = 0.6$ V. (c) The comparison of gate to drain capacitance versus gate voltage with different spacer materials.

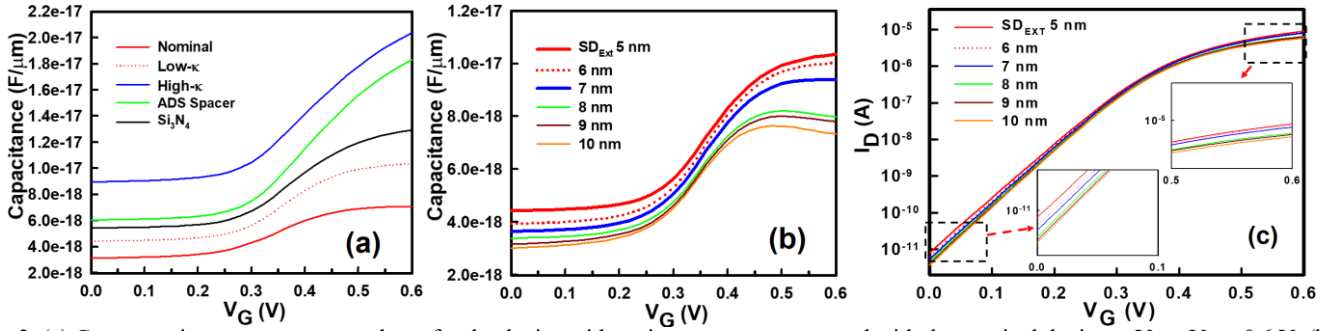

Fig. 3. (a) Gate capacitance versus gate voltage for the device with various spacers, compared with the nominal device at $V_D = V_G = 0.6$ V. (b) Gate capacitance versus gate voltage with the different S/D extensions of SiO_2 spacer. (c) I_D-V_G characteristic with different S/D extensions of SiO_2 spacer.

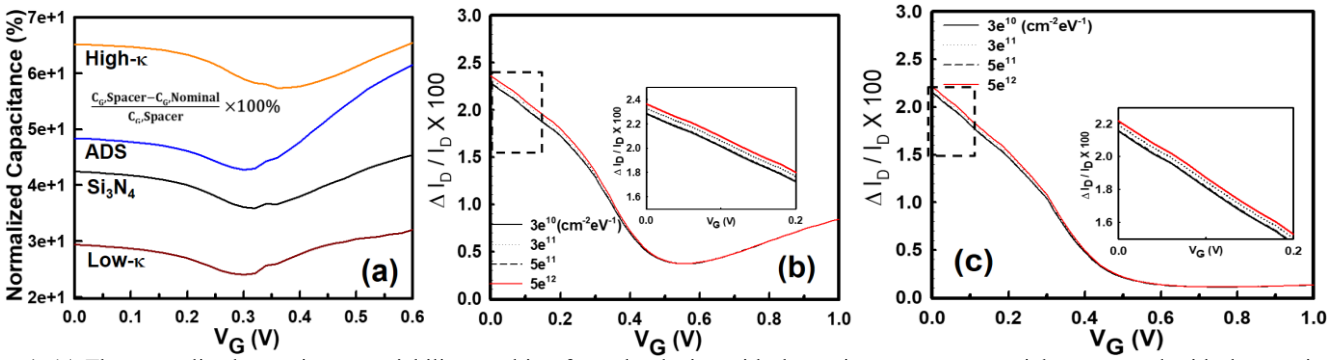

Fig. 4. (a) The normalized capacitance variability resulting from the device with the various spacers materials, compared with the nominal device. (b) The calculated amplitude of the RTN induced by the SCT locating at middle of the channel for nominal device under the biasing of $V_G = 1$ V and $V_D = 0.01$ V. Similarly, (c) is the device with ADS spacer. There is no significant change in SCT-induced RTN for the device with and without ADS.