

Low Temperature (<300°C) Fabrication of Ge MOS Structure for Advanced Electronic Devices

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Abstract

Ge has potential for novel electronic devices such as spintronics and flexible electronics. In order to realize such applications, device process should be designed with low temperature. In this study, we challenged to fabricate high quality Ge MOS capacitor at low temperature. Y₂O₃ and GeO₂ mixed compound (YGO) was selected as a gate dielectric material. Electron beam evaporated YGO with substrate heating showed superior C-V characteristics even at low annealing temperature of 300°C.

1. Introduction

Ge is of great interest in MOSFET applications due to its high carrier mobilities. Many issues have been solved, and high mobility Ge MOSFETs have been reported. [1,2] Another possible application ways of Ge are spintronics (spin-FET: Fig. 1(a)) and flexible electronics (high mobility Ge TFT on polymer substrate: Fig. 1(b)) [3,4]. For such applications, a low temperature fabrication process is necessary because of the low thermal stability of spin-source/drain or polymer substrate (spin-FET: spin S/D require process under 450°C, flexible-TFT: flexible substrate require process under 300°C). However, no one has focused fabrication of high quality Ge MOS at low temperature yet. In this study, we aim to investigate qualities of Ge MOS capacitors (CAPs) fabricated under low temperature (<300°C).

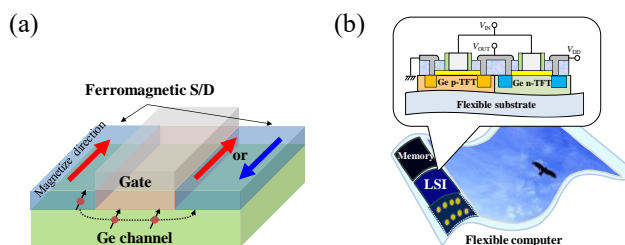


Fig. 1 Schematic images of (a) spin-FET and (b) flexible device on plastic substrate.

2. Experimental, Results and Discussion

In this study, we focused on Y₂O₃ and GeO₂ mixed compound (YGO) as a gate dielectric because it has been reported that this material showed excellent electrical characteristics as gate dielectric and good thermal and chemical stability on

Ge [5]. According to the previous research, YGO film was formed by PVD (sputtering) method and was annealed at 500°C, which is too high for our target application. Therefore, we tried to decrease the annealing temperature.

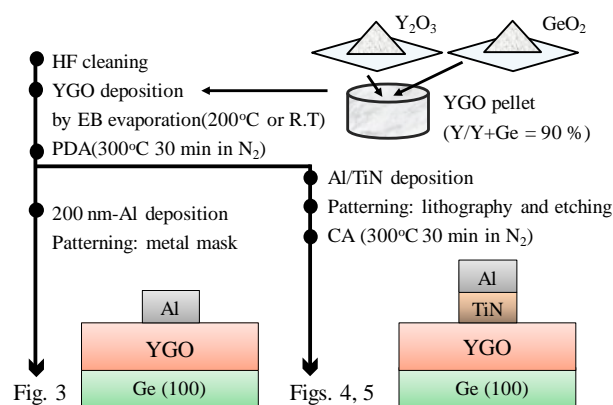


Fig. 2. Fabrication procedures for YGO MOSCAPs at low temperature.

First, we confirmed the substrate heating effect during YGO deposition. Figure 2 illustrates the MOSCAPs structure and fabrication processes. The Ge substrates were moderately doped (100) p- and n-Ge. After wet chemical cleaning of the substrate, 14 nm-YGO film was deposited by electron beam (EB) evaporation. We used pelletized evaporation source by pressing mixed powder of Y₂O₃ and GeO₂, and the atomic ratio of Y in Y+Ge was controlled to be 90%. Substrate temperature was set to RT or 200°C during YGO deposition. Then, post deposition annealing (PDA) was performed at 300°C for 30 min in N₂. Finally, Al electrode was formed through a metal mask with $\Phi=250\ \mu\text{m}$. Figure 3 shows deposition temperature dependence of the high-frequency (1 MHz) C-V characteristics. Even through the PDA temperature was relatively low, both samples showed typical MOS C-V curves. Narrower hysteresis (*HT*) was observed in the sample deposited at 200°C, which means lower border trap (slow trap) density in YGO film. Therefore, high temperature YGO deposition is effective to improve quality of gate dielectric.

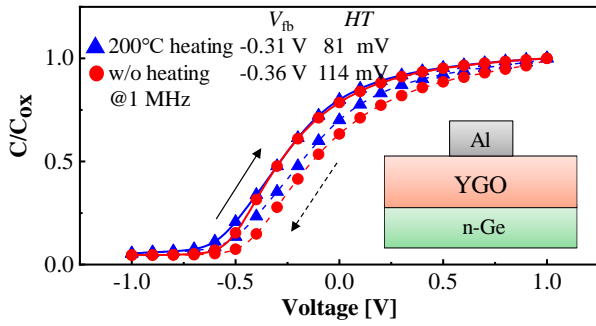


Fig. 3 C - V characteristics of Ge n-MOSCAPs with and without substrate heating during YGO deposition.

Considering application for novel devices, we fabricated MOSCAPs with TiN metal gate electrode. The fabrication details are also shown in Fig. 2. After PDA at 300°C, 25 nm-thick TiN and 200 nm-thick Al films were subsequently deposited by rf sputtering and thermal evaporation, respectively. The gate electrode was patterned into 150×150 μm^2 square by standard photolithography and wet etching technique. Finally, contact annealing was carried out at 300°C for 30 min in N_2 . The high-frequency C - V characteristics and frequency dependence of the MOSCAPs are shown in Figs. 4 and 5, respectively. They showed sharp C - V characteristics with small frequency dispersion. The equivalent oxide thickness (EOT) and effective dielectric constant (k) of YGO are estimated to be about 5 nm and 10.5, respectively. This k value is close to the experimental result of Y_2O_3 (12) [6]. Both n- and p-type MOSCAPs showed very narrow HT lower than 50 mV. It is reported Y atom effectively terminate dangling bond in YGO [5]. The energy distributions of interface state density (D_{it}) evaluated by deep level transient spectroscopy are shown in Fig. 6. They are comparable with the MOSCAPs with conventional $\text{SiO}_2/\text{GeO}_2$ gate dielectrics fabricated at the same temperature (300°C) [7].

3. Conclusions

For novel Ge applications, we fabricated Ge MOSCAPs at low process temperature under 300°C. The EB evaporated YGO with substrate heating showed superior characteristics as a gate dielectric. Ge MOSCAPs with TiN gate electrode and YGO gate dielectric showed very low HT and its D_{it} were comparable with conventional $\text{SiO}_2/\text{GeO}_2$ gate insulator. This material and process will be able to apply to the future novel Ge devices such as spin-FET and flexible Ge TFT.

References

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Acknowledgement

This work was partially supported by JSPS KAKENHI Grant (19K15028) and the cooperative Research Project Program of the RIEC, Tohoku University.

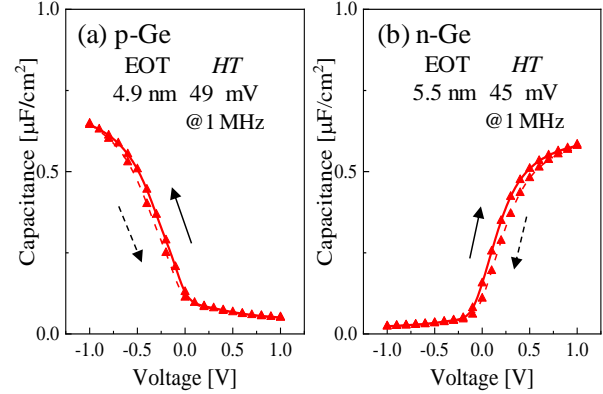


Fig. 4 High frequency C - V characteristics of the Al/TiN/YGO/Ge MOSCAPs (a) p-Ge and (b) n-Ge.

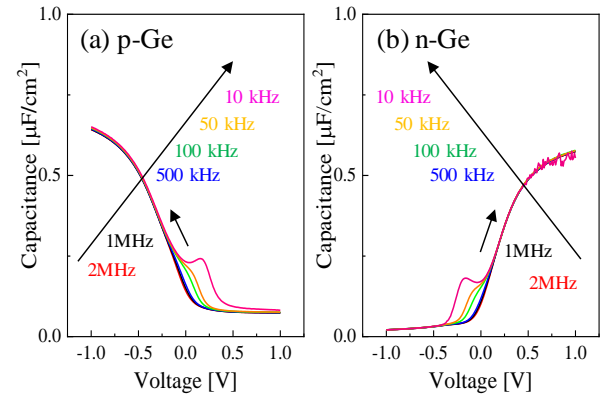


Fig. 5 C - V frequency dependence of the Al/TiN/YGO/Ge MOSCAPs (a) p-Ge and (b) n-Ge.

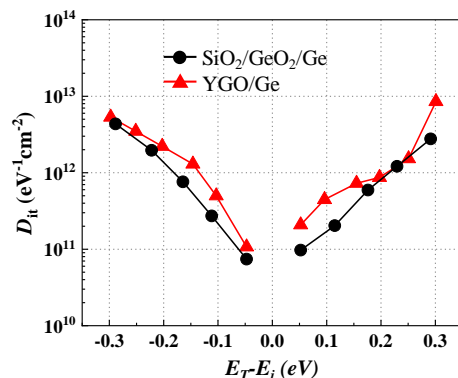


Fig. 6 D_{it} energy distributions of the Al/TiN/YGO/Ge MOSCAPs. For a comparison, D_{it} of Al/TiN/ $\text{SiO}_2/\text{GeO}_2/\text{Ge}$ are also shown.