Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp641-642

Ge nMOSFETs with GeO_x Passivation Formed by 450°C Oxygen RTA Postoxidation

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Abstract

In this work, Ge nMOSFETs were fabricated on p-Ge (001) with gate-last process. GeO_x passivation layer was formed by oxygen and ozone postoxidation using ~0.9nm Al_2O_3 as block layer. The impact of RTA temperature was investigated. Ge nMOSFETs with GeO_x formed by conventional 450°C oxygen RTA in 1 atm achieve the higher on-state current I_{ON} and steeper subthreshold swing (*SS*) as compared with the devices formed with 350°C and 400°C oxygen RTA. Ge nMOSFETs with 450°C exhibited the highest effective electron mobility of 522$cm^2/V{\cdot}s$. By comparing with our precious work, it is founded that oxygen RTA postoxidation is better for Ge nMOSFETs fabrication, while, ozone low pressure postoxidation by PEALD is better for Ge pMOSFETs.

1. Introduction

Germanium is considered as a promising candidate for future CMOS applications as channel materials for its higher electron and hole mobility [1]. Due to the challenge of passivation technique [2] and high contact resistance caused by Fermi-Level pinning [3], the report of Ge nMOSFETs is much less than Ge pMOSFETs. Otherwise, the high temperature needed in n-type impurity activation would cause a serious damage in the interface between Ge channel and dielectric [4]. Hence, a gate-last process is expected to achieve a higher performance.

In this work, Ge nMOSFETs with GeO_x passivation were fabricated. A 70 cycles Al_2O_3 in total was deposited by PEALD as gate dielectric. A 100nm sputtered TiN and NiGe alloy were used as gate metal and S/D contact, respectively. GeO_x was formed by ozone or oxygen postoxidation. And, a comparison study of the devices with three different RTA temperature is performed. It should be noted that in our previous work [5], Ge pMOSFETs with ozone postoxidation works well, but in this work, it is observed that an oxygen based postoxidation is better for Ge nMOSFETs.

2. Device Fabrication

The device structure and key process flow of gate-last Ge nMOSFETs are schematically shown in Fig. 1. P type Ge (001) with a resistivity of 0.136-0.182 Ω·cm was used as the starting substrate. Firstly, mesa and alignment mark were patterned and dry etched by RIE. P^+ ion implantation with an energy of 30keV and a dose of 1×10^{15} cm^{-2} was performed into the exposed S/D region. RTA treatment with 600°C in N_2 for 30s was carried out for P^+ doping activation. After that, the wafer was carefully cleaned by acetone, plasma asher and diluted HF. Then the wafer was immediately transferred into PEALD chambers followed by 10 cycles Al_2O_3 deposition at 300°C. The thickness of 10 cycles Al_2O_3 was estimate to be 0.9 nm experimentally. After that, half of the wafer was treated by ozone at 300°C for 15 minutes in PEALD chamber while another half was transferred into RTA chambers and treated by O_2 at 450°C for 15min. 60 cycles Al_2O_3 was than deposited for each wafer and the thickness was estimate to be 5.4 nm. About 100nm TiN was than deposited by magnetron sputtering followed by lithography and dry etching. To form the S/D contact, 25nm Ni was deposited by e-beam evaporation and lift-off process. Finally, RTA was carried out at 350°C, 400°C or 450°C.

3. Results and Discussion

Fig. 2 (a) shows the I_D and I_S *vs.* V_{GS} of the fabricated Ge nMOSFETs with GeO_x passivation oxidized by oxygen and ozone. The gate length/width is 4μm/100μm and RTA temperature is 450°C. Ge nMOSFETs with ozone postoxidation achieve a lower on-state current and a *SS* of 249mV/decade in comparison with the devices formed with O_2 postoxidation in which the *SS* is 122mV/decade. 4 times higher I_D is achieved in the O_2 passivated devices at V_{GS} - V_{TH} = 0.8V as compared with the ozone passivated device as shown in Fig. 3(b). The enhanced current and *SS* characteristics for the O_2 passivated device identified that O_2 postoxidation is a promising passivation for Ge nMOSFET fabrication.

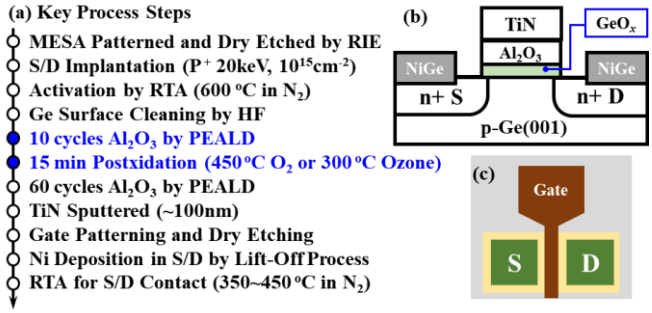

Fig. 1. (a) Key process steps of the Ge pMOSFETs fabrication and device structure shown in (b) cross-section and (c) top view.

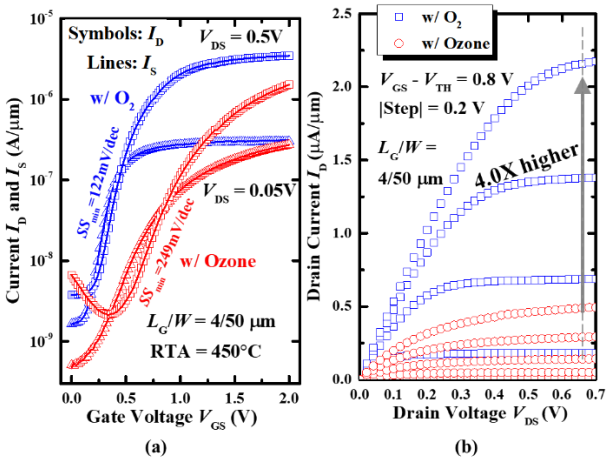

Fig. 2. (a) I_D and I_S *vs.* V_{GS} curves and (b) I_D *vs.* V_{DS} of Ge nMOSFETs by O_2 or ozone postoxidation.

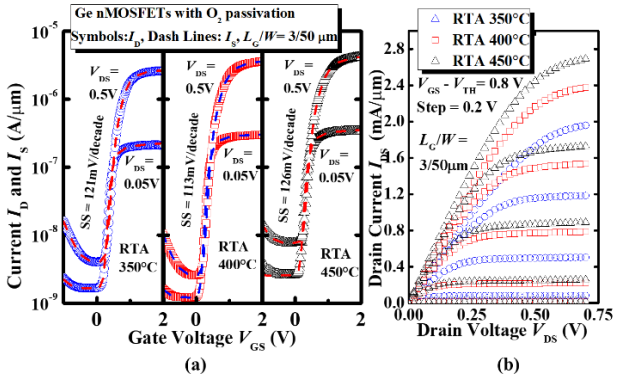

Fig. 3. (a) I_D and I_S *vs.* V_{GS} curves and (b) I_D *vs.* V_{DS} of Ge nMOSFETs by

O_2 postoxidation with different RTA temperature range from 350℃ to 450℃.

Fig. 3(a) shows measured transfer characteristics of Ge nMOSFETs with O_2 postoxidation passivation, annealed at 350℃, 400℃ and 450℃. The gate length L_G and gate width W are 3μm and 50 μm, respectively. The devices treated by 450℃ RTA exhibit a higher drain current I_D than the devices annealed at 350 ℃ and 400 ℃. The I_D *vs.* V_{DS} curves shown in Fig.3 (b) also demonstrate a significant improvement of I_D at V_{GS}-V_{TH} = 0.8 V and V_{DS} = 0.7 V for Ge nMOSFETs annealed at 450 ℃. Here in this work, threshold voltage is defined as the corresponding V_{GS} when $g_m = \partial I_{DS}/\partial V_{GS}$ get the peak value. The improved I_{DS} at higher RTA temperature is attributed to the decreased S/D resistance (R_{SD}) and improved effective mobility μ_{eff}, which will be proved later.

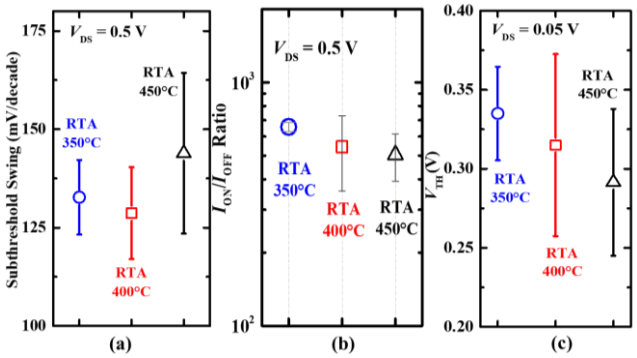

Fig. 4. (a)*SS* (b) I_{ON}/I_{OFF} ratio and (c) V_{TH} distribution of Ge nMOSFETs.

Fig. 4 summarized the *SS*, I_{ON}/I_{OFF} ratio, and V_{TH} of Ge nMOSFETs annealed at three temperatures. Each point in Fig. 4 was measured for more than 6 transistors and error bar was added to show the randomness. As shown in Fig. 4(a), the devices annealed at 350℃ and 400℃ has a lower *SS* than the devices annealed at 450℃. Fig. 4(b) shows that I_{ON}/I_{OFF} ratio reduced with the annealing temperature increased. And in Fig. 4(c) V_{TH} also shifts to the negative direction. This might be due to the interface traps increase caused by the higher annealing temperature.

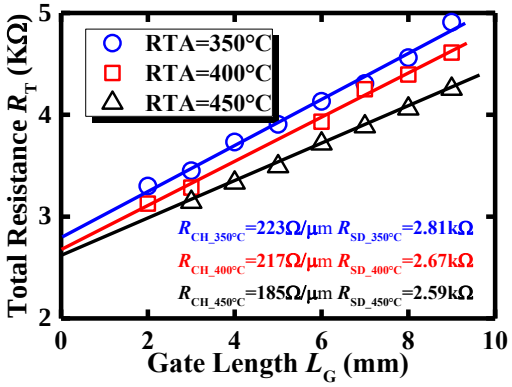

Fig. 5. R_T *vs.* L_G of Ge nMOSFETs with GeO_x passivation measured at V_{GS} - V_{TH} = 0.8V and V_{DS} = 0.05V.

The total on-state resistance (R_T) of Ge nMOSFETs were measured at V_{GS} - V_{TH} = 0.8V and V_{DS} = 0.05V and plotted as a function of L_G as shown Fig.5. The S/D series resistance R_{SD} and channel resistance R_{CH} can be deduced from the y-intercept and slope of this plot, respectively, which is shown as the insertion of Fig.5. It can be seen that both R_{SD} and R_{CH} are reduced with the annealing temperature increased. The devices with 450℃ annealing have a R_{CH} of 185Ω/μm and R_{SD} of 2.59 kΩ. The R_{SD} may further reduced by various Femi-Level depinning treatment.

Fig. 6 shows the behavior of Gate to source capacitance C_s versus V_{GS} measured at frequency of 100kHz. The improvement of C_s may caused by the crystallization of Al_2O_3 on high temperature and this could also reduce the equivalent oxide thickness, improve the I_{ON}.

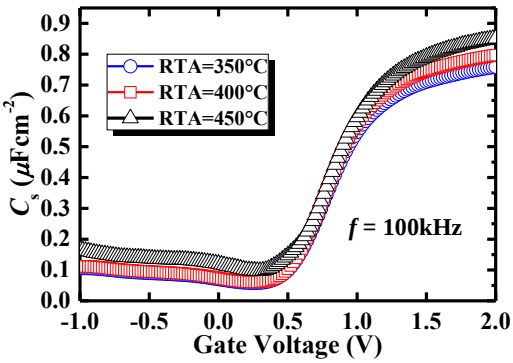

Fig. 6. Gate to source capacitance C_s *vs.* V_{GS} characteristics measured at a frequency of 100 kHz.

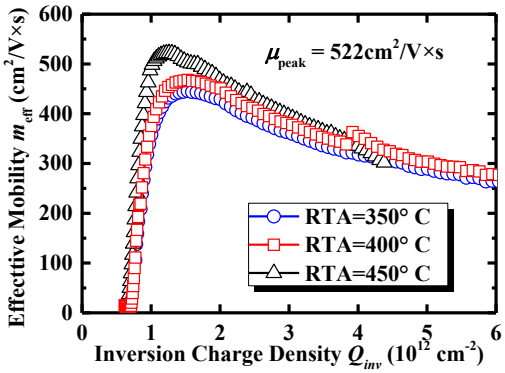

Fig. 7. Effective electron mobility μ_{eff} as a function of inversion charge density Q_{inv} deduced by a split *C-V* method.

In Fig.7 μ_{eff} versus Q_{inv} of these devices are extracted by a split *C-V* method [6], demonstrating that Ge nMOSFETs with RTA of 450℃ achieves higher peak electron mobility of 522cm^2/V·s than the transistors with lower annealing temperature. The peak of this three curves have an approximate same Q_{inv}, identified a similar surface roughness scattering.

4. Conclusions

The impact of oxidation by ozone or O_2 on Ge nMOSFETs passivated by GeO_x are investigated. When compared with ozone oxidation, I_{DS}-V_{GS} and *SS* characteristic can be obviously enhanced by using O_2 RTA oxidation. For the devices with O_2 oxidation, a 450℃ final RTA in N_2 can reduce both the channel and S/D resistance, improves the I_{ON} and μ_{eff}.

Acknowledgments. G. Han acknowledges support from the National Natural Science Foundation of China (Grant No. 61534004).

References

[1] A. Toriumi *et al*., Jap. J. Appl. Phys. **57** (2017) 010101.

[2] C. H. Lee *et al*., IEDM (2011) 18.1.1.

[3] T. Nishimura *et al*., Appl. Phys. Lett. **91** (2007) 123123.

[4] K. Kita *et al*., Jap. J. Appl. Phys. **47** (2008) 2349.

[5] Y. Xu *et al*., Nano. Res. Lett. **14** (2019) 126

[6] G. Niu *et al*., IEEE TED. **46** (1999) 1912.