Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp647-648

A Junctionless SOI FET with Channel Thinning by Ion Implantation (CTIFET) and its application to 6T-SRAM Cell

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Abstract

In this study, a junctionless (JL) SOI FET with channel thinning via ion implantation (CTI), called CTIFET, is proposed for the first time and its application to 6T-SRAM is presented. Simulation results reveal that the proposed device with the original channel thickness (T_{ch}=25 nm) effectively reduced by an implanted counter doping region could effectively increase on-state current, suppress off-state leakage current (I_{off}), and reduce subthreshold swing (SS) by about 3.4%, 81%, and 3.2%, respectively, as compared with those of conventional UTBFET and recessed channel FET (RCFET) with T_{ch}=10 nm. In addition, the CTIFET-based 6T-SRAM shows an SNM at V_{dd}=1.2 V as high as 228 and 461 mV during read and write operation, respectively. The best read stability (RSNM) and write stability (WSNM) are 291 mV at a cell ratio (CR) of 2.5 and 377 mV at PR=3, respectively. An enhancement in the writing mode performance by about 15.6% is obtained. The improvements in device and 6T-SRAM performances are attributed to the considerable harvest of gate control originating from channel thinning through ion implantation.

1. Introduction

Channel thickness is one of the key parameters in gate controllability of UTBFET and FinFET [1-2]. SOI wafers with thin enough Si thickness (e.g., t_{Si} < 20 nm) are still quite expensive nowadays and the thickness uniformity remains a tough challenge especially for $t_{Si} \leq$ 10 nm. Recessed channel (RC) through a precise etching or oxidation-thinning process has been successfully demonstrated for UTBFET devices [3], but it leaves an uneven surface around the channel region. In this study, a simple ion-implantation channel thinning (CTI) method is proposed to promote junctionless (JL) FET performance with the surface morphology of channel region keeping intact. Via precise control of the projection range and straggle of the implanted region at the bottom of channel layer, thick SOI wafer (e.g., t_{Si} = 25 nm) could be served as a thin one with an effective $t_{Si} \leq$ 10 nm. The influence of ion implantation parameters on the electrical properties of the proposed CTIFET using 25 nm thick SOI wafer is investigated. Comparisons of the performance of devices and application to 6T static random access memory (SRAM) based on conventional UTBFET and RCFET with 10 nm thick channel layer and CTIFET using 25 nm thick SOI wafer are made and discussed.

2. Proposed device structure

Fig.1 shows the proposed device structure of the proposed CTIFET and the ion implantation processing parameters used in the simulation. Based on SOI wafers with both the Si layer (n-type) and buried oxide layer (BOX) have the same thickness of 25 nm, boron (B) implantation is performed with the dosage, energy, angle of implantation, and rotation times of the wafer serving as process parameters. Through a precise control of projection range, straggle and doping concentration of the implanted region with a counter doping at the bottom of channel layer, an effective n-region with a thickness (T_{ch}) ranging from 5 to 10 nm, depending on the thickness of the implanted region and depletion region, which is necessary for JL CTIFET to realize fully depleted channel. Accordingly, a considerable enhancement in gate controllability can be expected. In addition, the implanted region could effectively block leakage current via a built-in potential between the internal region and n-Si, a reduced off-state leakage current can also be achieved.

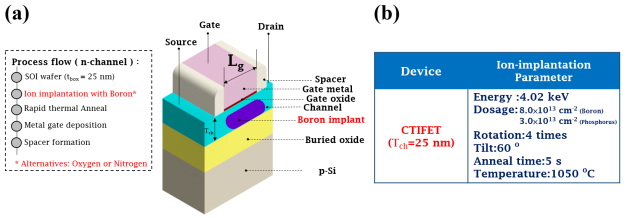

Fig. 1 (a) Process flow and schematic of the proposed CTIFET. (b) Ion implantation processing parameters used in the simulation.

Sentaurus TCAD tool considering quantum confinement effects was employed in this study. Fig. 2 shows the device structures and Table I highlights the key structural parameters used in the simulation. Note that UTBFET and RCFET with the same 10 nm thick channel are also simulated for comparison. All devices have the same gate length of 90 nm, EOT of 3 nm, and threshold voltage of 0.5 V. The transfer curves of device at V_{dd}=50 mV and 1.2 V are used for DIBL evaluation.

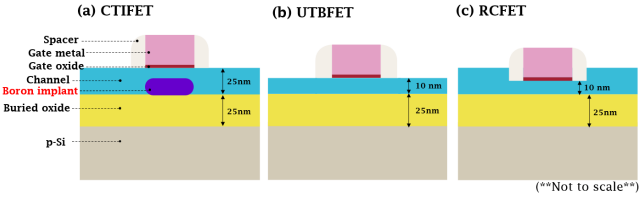

Fig. 2 Key structural parameters used for the simulation and performance comparisons. (a) CTIFET, (b) UTBFET, and (c) RCFET.

Table I Device design parameters used in the simulation.

Parameter	Symbol	CTIFET	UTBFET	RCFET
Supply Voltage (V)	V_{dd}	1.2	1.2	1.2
Low drain voltage (V)	$V_{d\text{-}Low}$	0.05	0.05	0.05
Channel Length (nm)	L_g	90	90	90
Channel Thickness (nm)	T_{ch}	25	10-25	10
Buried Oxide Thickness (nm)	t_{box}	25	25	25
Equivalent Oxide Thickness (nm)	t_{ox}	3	3	3
Source/Drain doping (cm^{-3})	N	10^{19}	10^{19}	10^{19}
Channel doping (cm^{-3})				

3. Simulation result and discussion

Fig. 3 (a) shows the effect of the boron implantation angle on the shape and contour of the implanted region, which play an important role in determining the short channel behaviors of CTFET. Fig. 3 (b) shows the effect of dosage of B implantation on the transfer characerisitcs of CTIFET, which decides the span of the depletion region beneath the n-Si channel and affects devcice performance.

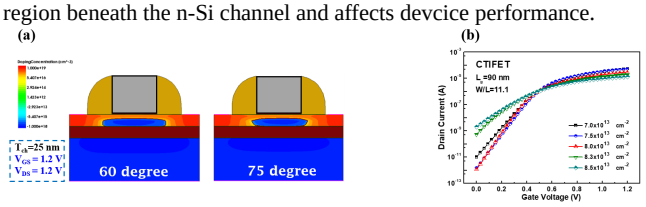

Fig. 3 (a) The effect of the boron implantation angle on the distribution of the implanted region and (b) the influence of dosage on the transfer characteristics of CTIFET.

Fig. 4 shows the calculated transfer I-V curves of CTIFET (based on T_{ch}=25 nm SOI wafer and with the ion implantation processing parameters shown in Fig. 1 (b)), UTBFET (for T_{ch}=25 nm and 10 nm case), and RCFET(T_{ch}=10 nm). Table II lists the corresponding electrical parameters. With the doping concentration of the n-Si keeps at 1×10^{19} cm^{-3}, it reveals that the gate control of UTBFET (T_{ch}=25 nm) is poor in which the channel can not be turned off. Comparable are found for all devices, nevertheless, CTIFET shows a considerably reduced I_{off} and improved SS and DIBL. It confirms the effectiveness of the implanted-channel in suppression off-state leakage current and enhancement in device performance, which could be very beneficial for SOI FETs using cost effective SOI wafers.

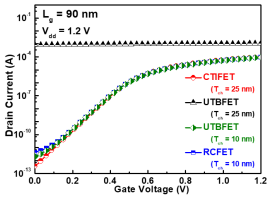

Table II The electrical parameters of CTIFET, RCFET, and UTBFET

Structure	T_{ch} (nm)	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}	SS (mV/dec)	DIBL (mV/V)
UTBFET	25	1.09×10^{-5}	8.50×10^{-6}	1.28	-	-
	10	9.15×10^{-5}	1.20×10^{-12}	7.63×10^{7}	75.4	43.5
RCFET	10	9.07×10^{-5}	4.18×10^{-12}	2.17×10^{7}	76.1	44.3
CTIFET	25	9.43×10^{-5}	3.51×10^{-13}	2.69×10^{8}	73.4	50.4

Fig. 4 Comparison of the calculated transfer I-V characteristics of CTIFET, RCFET, and UTBFETs.

According to the structural parameters outlined in Fig. 1 and Table I, p-channel devices were also simulated and their applications to 6T-SRAM were performed. Note that phosphorus (P) was used for the implantation for CTIFET with the different dosage of n-CTIFET and appropriate implantation parameters. Fig. 5 shows the influence of V_{dd} on the read and write static noise margin (SNM) of the SRAM based on CTIFET. SNMs as high as 228 and 461 mV for the read and write operation, respectively, are achieved which indicates a high stability of the 6T-SRAM [6-7]. Here SNM was calculated using a butterfly curve method, which decreases with decreasing V_{dd} for reduced I_{on}.

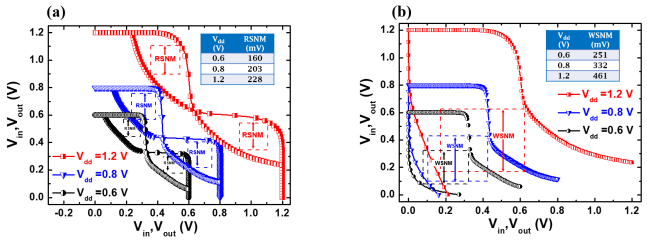

Fig. 5 Effect of different V_{dd} of CTIFET based on 6T-SRAM cell for (a) Read SNM (b) Write SNM.

Fig. 6 shows the effect of WL voltage (VWL) on the SNM of 6T-SRAM based on CTIFET. It is found that VWL is continuously reduced during write operation, but not for the written operation. Hence, for data to be safely written, the VWL should keep ≥ $0.8V_{dd}$. To increase SNM and, in turn, enhance the stability of 6T-SRAM cell, trade-off between the performances of read and write operations should be made. Essentially, V_{dd} should be maximized for read/write operation, while VWL should keep as low as possible for read operation.

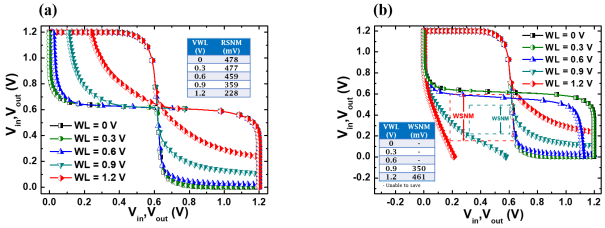

Fig. 6 Effect of VWL on SNM of 6T-SRAM based on CTIFET. (a) Read SNM (b) Write SNM.

Transistor sizing modulation is usually used to enhance SNM. The influence of cell ratio (CR) and pull up ratio (PR) on the stability of the 6T-SRAM cell is also examined. To keep the cell area within reasonable values, CR values in the range of 1-2.5 and PR in the range of 3-4 are considered. Fig. 7 shows the simulation results of 6T-SRAM based on CTIFET. It shows that RSNM (Fig. 7 (a)) increases with increasing CR and an inverse situation is found for increasing PR (Fig. 7 (b)), indicating a trade-off between read and write operation.

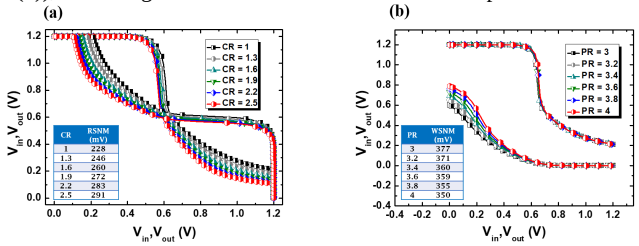

Fig. 7 Effect of transistor sizing of 6T-SRAM based on CTIFET. (a) CR (b) PR.

Table III Key electrical parameters of 6T-SRAM based on CTIFET, RCFET and UTBFET

Structure	T_{ch} (nm)	RNM (mV)	WNM (mV)	I_{CRIT_RD} (μA)	I_{CRIT_WR} (μA)
CTIFET	25	228	461	69.7	80.5
RCFET	10	232	375	76.2	76.3
UTBFET	10	235	378	75.6	64.1

A comparison of the 6T-SRAM performance among all the FETs considered in this work was also made. The key performance parameters of 6T-SRAM based on UTBFET (T_{ch}=10 nm), RCFET (T_{ch}=10 nm), and the proposed CTIFET (T_{ch}=25 nm) are listed in Table III. It reveals that the CTIFET based 6T-SRAM cell provides comparably good performance but with a much better stability under the write operation. An improvement in writing mode by about 15.6 % is achieved.

4. Conclusions

The use of ion-implantation for channel thinning of JLSOI FETs and 6T-SRAM have been demonstrated. Simulation results have confirmed the effectiveness of the implanted-channel in suppression off-state leakage current and enhancement in device performance attributing to an effective channel thinning. Through using SNM as a measure of the stability during read/write operations, 6T-SRAM based on the proposed CTIFET with a significantly increase in the write mode SNM by about 15.6 % has been achieved. The proposed CTIFET is expected to be a promising candidate for 6T-SRAM fabricated on cost-effective thick SOI wafers, which could make possible a jumping for serval technology nodes for conventional SOI FETs.

Acknowledgements

This work was supported by the Ministry of Science and Technology (MOST), Taiwan, under contract no. MOST 105-2221-E-006-196-MY3.

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