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Theoretical Investigation of Performance Improvement in GeSn/SiGeSn TFET with Double Type-II Staggered Heterojunction

Yang Xu, Hongjuan Wang, Genquan Han*, Yan Liu and Yue Hao
Wide Bandgap Semiconductor Technology Disciplines State Key Laboratory, School of Microelectronics, Xidian University, China.
*Email: hangenquan@ieee.org

Abstract

We demonstrate the performance improvement in GeSn/SiGeSn hetero tunneling field-effect transistor with double type-II heterojunction (DH-TFET) in which the $Si_{0.47}Ge_{0.33}Sn_{0.20}/Si_{0.24}Ge_{0.62}Sn_{0.14}$ type-II heterojunction located in channel region via numerical simulation. The DH-TFET achieves the higher on-state current (I_{ON}) and the steeper subthreshold swing (SS) as compared with the GeSn homo-TFET and conventional GeSn/SiGeSn hetero-TFET devices. The performance enhancement is mainly owing to the larger carrier density inside of the region between two heterojunction in DH-TFET attributing to the presence of $Si_{0.47}Ge_{0.33}Sn_{0.20}/Si_{0.24}Ge_{0.62}Sn_{0.14}$ heterojunction located in channel region.

1. Introduction

The tunneling FET (TFET) is considered as a promising device for ultralow power consumption applications [1]-[2]. But, TFET device is still facing one key challenge that is the insufficient on-state current (I_{ON}) as compared with MOSFET. GeSn has attracted tremendous research interests for TFET design owing to the easy integration on Si and the ability that can achieve direct BTBT by increasing Sn composition thus enhancing the BTBT efficiency [3]-[6]. However, due to the limitation of solid solubility of Sn in Ge, the Sn composition cannot increase arbitrary. Hence, GeSn based hetero-TFET has been investigated and traditional lattice-matched GeSn/SiGeSn hetero-TFET with improved device performance than GeSn homo device has been reported [7].

In this work, to further improve the device performance, lattice-matched GeSn/SiGeSn hetero-TFET with double type-II staggered heterojunction (DH-TFET) are designed and characterized by numerical simulation. As the double type-II hetero junction applied, the I_{ON} and SS improvement of GeSn/SiGeSn DH-TFET is demonstrated owing to the slightly smaller tunneling barrier and the larger carrier density in tunneling region attributing to the second type-II staggered heterojunction located in channel.

2. Device Design and Simulation Methodology

The schematic of GeSn/SiGeSn hetero-TFET and DH-TFET with key device parameters is shown in Fig. 1(a). In traditional GeSn/SiGeSn hetero-TFET, lattice-matched $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ was used to form the type-II staggered tunneling junction (TJ) with the conduction and valence band offsets of 29.8 and 162 meV, respectively, and $Si_{0.47}Ge_{0.33}Sn_{0.20}$ was utilized to form channel and drain region as shown in Fig. 1(b). While, in DH-TFET, beside the $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ TJ, the lattice-matched $Si_{0.47}Ge_{0.33}Sn_{0.20}/Si_{0.24}Ge_{0.62}Sn_{0.14}$ was employed to form the second heterojunction with the conduction and valence band offsets of 149 and 81 meV, respectively, in channel region [Fig. 1(c)]. The length of $Si_{0.47}Ge_{0.33}Sn_{0.20}$ in DH-TFET is defined as l. The $Ge_{0.92}Sn_{0.08}$ homo-TFET was also considered as control device.

The electrical performance of homo- and hetero-TFETs was computed using the 2-D self-consistent simulations with Sentaurus TCAD simulator in which the dynamic nonlocal tunneling algorithm was employed. BTBT was calculated based on Kane's model [8]. Quantum confinement effect was considered by utilizing the density gradient quantization model [9]. The Key parameters of GeSn and SiGeSn used during the simulation was obtained from Ref. [7].

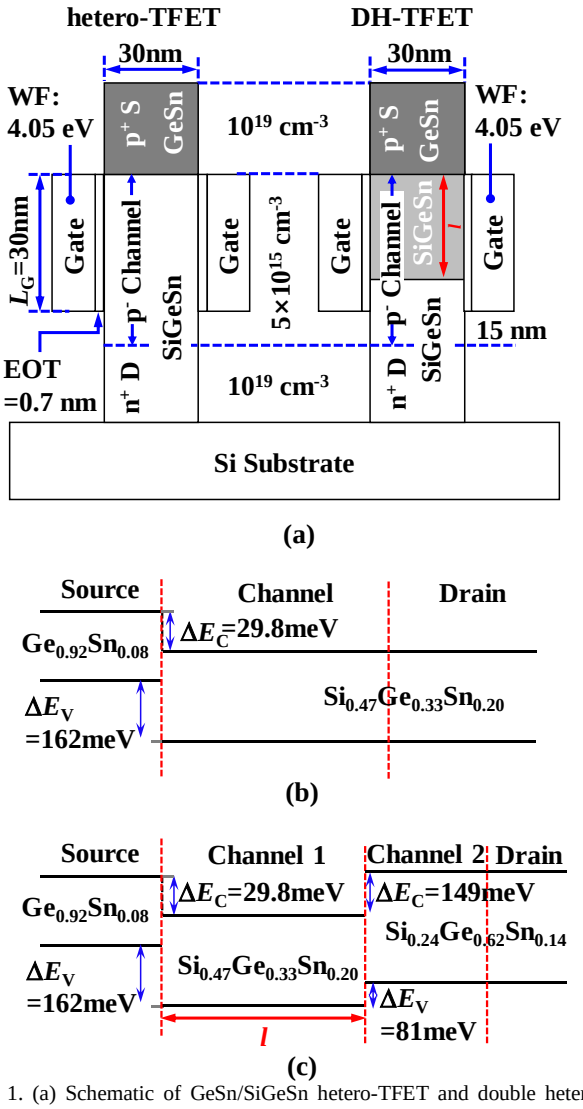

Fig. 1. (a) Schematic of GeSn/SiGeSn hetero-TFET and double heterojunction TFET (DH-TFET) on Si. The schematics of band alignment of (b) $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ hetero-TFET and (c) $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}/Si_{0.24}Ge_{0.62}Sn_{0.14}$ DH-TFET.

3. Electrical Results and Discussion

The calculated I_{DS}-V_{GS} curves of $Ge_{0.92}Sn_{0.08}$ homo-TFET, $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ hetero-TFET and $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}/Si_{0.24}Ge_{0.62}Sn_{0.14}$ DH-TFET at V_{DS} of 0.3V are shown in Fig. 2. Here, the l in DH-TEFT is 10nm. The DH-TFET demonstrates the larger onset voltage V_{ONSET}, but the sharper turn-on characteristic and the enhanced drive current as compared with the two control devices. It can be observed that, at V_{GS}=0.5V, the DH-TFET achieves 1.35X higher current as compared with traditional hetero-TFET.

Fig. 3(a) shows the point SS extracted from Fig. 2 as a function of I_{DS} for homo-, hetero- and DH-TFETs. Point SS obtained at each V_{GS} is defined as $dV_{GS}/d(\log I_{DS})$. The higher maximum I_{DS} with sub-60 mV/decade SS is achieved in DH-TFET over the control devices. $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}/Si_{0.24}Ge_{0.62}Sn_{0.14}$ DH-TFET demonstrates a sub-60 mV/decade SS over almost six

decades of I_{DS}, which is superior to the $Ge_{0.92}Sn_{0.08}$ homo-TFET, $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ hetero-TFET. The I_{ON} *vs.* I_{OFF} characteristics for the devices, as the crucial factors determining the performance of the TFETs are shown in Fig. 3(b). I_{ON} is extracted at V_{GS}-V_{OFF}=V_{DS}=0.3V, where V_{OFF} is the voltage at which I_{DS}=I_{OFF}. At a fixed I_{OFF}, DH-TFET demonstrates higher I_{ON} and I_{ON}/I_{OFF} as compared with the hetero- and homo-TFETs. At I_{OFF}=10^{-11}A/μm, the I_{ON} of DH-TEFT is 1.8 times higher than the conventional hetero-TFET. It can also be seen that I_{ON} of DH-TFET exhibits less sensitivity to I_{OFF} than that of hetero- and homo-TFETs, which is owing to the improved *SS* characteristics [Fig. 3(a)].

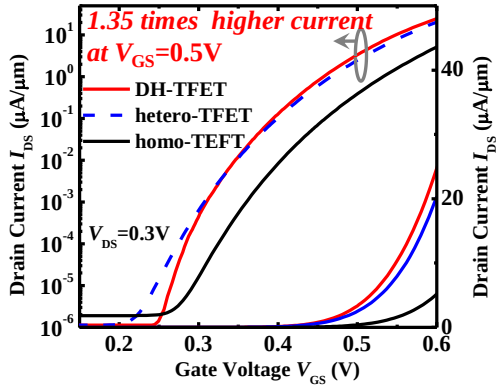

Fig. 2. $Ge_{0.92}Sn_{0.08}$ homo-TFET, $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ hetero-TFET and $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}/Si_{0.24}Ge_{0.62}Sn_{0.14}$ DH-TFET at V_{DS} of 0.3V.

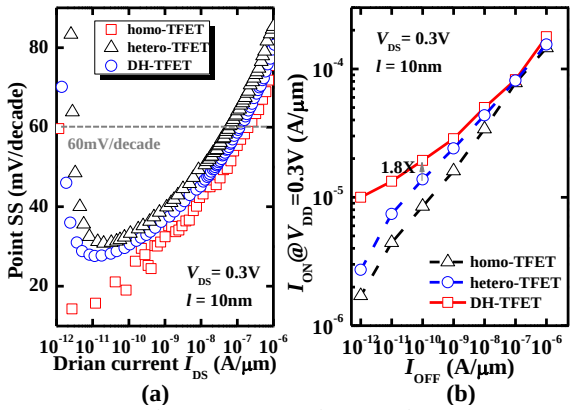

Fig. 3. Comparison of (a) Point *SS* as a function of I_{DS} and (b) I_{ON} *vs.* I_{OFF} for $Ge_{0.92}Sn_{0.08}$ homo-TFET, $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ hetero-TFET and $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}/Si_{0.24}Ge_{0.62}Sn_{0.14}$ DH-TFET at V_{DD} = 0.3 V. V_{OFF} is defined as V_{GS} where I_{DS} is equals the values of given I_{OFF}, and I_{ON} is extracted at V_{GS}–V_{OFF} = V_{DS} = 0.3V.

To illustrate the boosting effect of the double type-II heterojunction, the energy band diagram and carriers density along channel direction for $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ hetero-TFET $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}/Si_{0.24}Ge_{0.62}Sn_{0.14}$ DH-TFET at V_{GS}=0.54V, V_{DD}=0.3V are plotted in Fig. 4. It can be observed that, compared with the conventional hetero-TFET, the DH-TFET achieves slightly shorter tunneling barrier [Fig. 4(a)]. Meanwhile, at same V_{GS}, the magnitude of carrier density located in the region between two heterojunction is much larger in DH-TFET than that in conventional hetero-TFET due to the presence of the $Si_{0.47}Ge_{0.33}Sn_{0.20}/Si_{0.24}Ge_{0.62}Sn_{0.14}$ heterojunction in channel region contributing to the enhanced tunneling efficiency thus the drive current (Fig. 2).

Besides, the impact of double type-II heterojunction on BTBT of devices is further analyzed by plotting the distribution of carrier generation rate G_{BTBT} (Fig. 5), which directly determines the magnitude of tunneling current. At V_{GS}=0.54V, V_{DD}=0.3V, the electron G_{BTBT} of $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}/Si_{0.24}Ge_{0.62}Sn_{0.14}$ DH-TFET are all located in the region between two heterojunction contributing to larger tunneling current as compared with $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ hetero-TFET.

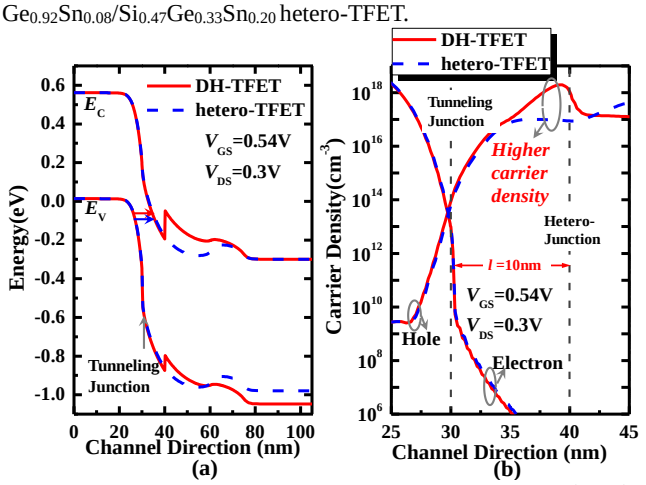

Fig. 4. (a) Energy band diagram and (b) Carrier density profiles for $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ hetero-TFET and $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}/Si_{0.24}Ge_{0.62}Sn_{0.14}$ DH-TFET at V_{GS}=0.54V, V_{DD}=0.3V.

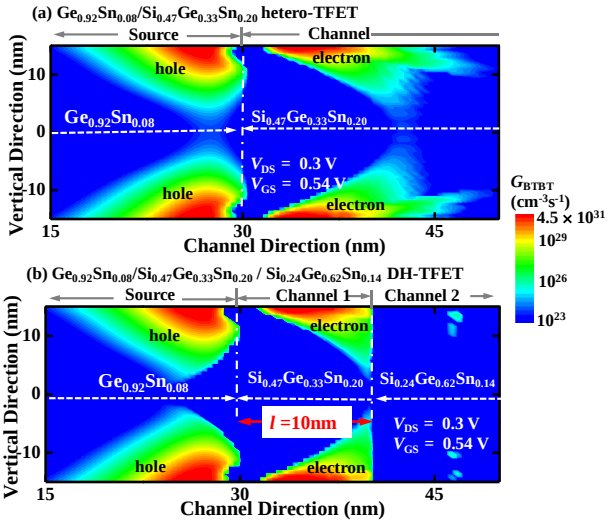

Fig. 5. Spatial distributions of G_{BTB} for (a) $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ hetero-TFET and (b) $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}/Si_{0.24}Ge_{0.62}Sn_{0.14}$ DH-TFET at V_{GS}=0.54V, V_{DD}=0.3V.

5. Conclusions

$Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}/Si_{0.24}Ge_{0.62}Sn_{0.14}$ DH-TFET is designed and investigated. It is demonstrated that the DH-TFET achieves sharper turn-on characteristic and higher tunneling current than the $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ hetero-TFET owing to the larger magnitude of carrier density and all the electron G_{BTBT} located in the region between two heterojunction attributing to the $Si_{0.47}Ge_{0.33}Sn_{0.20}/Si_{0.24}Ge_{0.62}Sn_{0.14}$ heterojunction in channel.

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