Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp653-654

# Scalability and $V_{th}$ Sensitivity Assessment of Core-Shell Junctionless MOSFET

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**Abstract**

**A semi-analytical model is presented to explore gate length ($L_g$) scalability and threshold voltage ($V_{th}$) sensitivity of a Core-Shell (CS) Junctionless (JL) MOSFET. Results indicate that CS JL device with shallow shell depth ($d$) exhibits excellent scalability (down to 10 nm) at shell doping ($N_d$) of $10^{19}$ cm$^{-3}$ with suppressed $V_{th}$ roll-off. A CS JL MOSFET with $d$ = 3 nm shows nearly 5×, 3× and 1.5× reduced $V_{th}$ sensitivity towards silicon film thickness ($T_{si}$), $N_d$ and $L_g$ variations, respectively, as compared to a conventional JL MOSFET.**

## 1. Introduction

The experimental demonstration of sub-5 nm shell doping profile (SDP) with abruptness less than 0.8 nm/dec in Junctionless (JL) transistor [1], [2] has renewed interest of the scientific community as higher on-to-off current ratio, improved Subthreshold swing ($S$) and reduced threshold voltage ($V_{th}$) variability has been achieved. The Core-Shell (CS) JL architecture has been examined for the impact of SDP on its electrical characteristics [3], mobility performance [4] and DRAM operation [5]. This work investigates scalability and $V_{th}$ sensitivity in CS JL devices through a semi-analytical approach to present design guidelines for optimal low voltage ($V_{ds}$ = 0.5 V) performance.

## 2. Modeling Approach, Validation and Discussion

As indicated in Fig. 1, the potential distribution $\phi(x,y)$ in the silicon film of CS JL MOSFET operating in subthreshold regime is governed by region-specific 2-D Poisson's equations, whose solutions are obtained by assuming separate parabolic potentials [6], and appropriate boundary and continuity conditions along the vertical ($y$-) direction in the three regions $R_1$, $R_2$ and $R_3$. The differential equations at the location of subthreshold conduction (i.e. $y = T_{si}/2$) [7] for different regions are obtained as

$$d^2\phi_{R1,R3}(x)/dx^2 = -qN_{eff}/\varepsilon_{si} \quad (1)$$

$$d^2\phi_{R2}(x)/dx^2 = (\phi_{R2}(x) - \phi_L)/\lambda \quad (2)$$

where $$N_{eff} = N_0 + (N_d - N_0)(2d/T_{si}) \quad (3)$$

$$\lambda = \sqrt{\left(4\varepsilon_{si}T_{si}T_{ox} + \varepsilon_{ox}T_{si}^2\right)/8\varepsilon_{ox}} \quad (4)$$

$$\phi_L = V_{gs} - V_{fb} + [qN_d(2d) + qN_0(T_{si} - 2d)]/2C_{ox} + \left[qN_d(4d^2) + qN_0\left(T_{si}^2 - 4d^2\right)\right]/8\varepsilon_{si} \quad (5)$$

On solving (1) and (2) simultaneously for $R_1$, $R_2$ and $R_3$ using the lateral boundary and continuity conditions [7], [8], the following solutions for channel potential is obtained as

$$\phi_{R1}(x) = V_{bi} - qN_{eff}(x + d_S)^2/\varepsilon_{si} \quad (6)$$

$$\phi_{R3}(x) = V_{bi} + V_{ds} - qN_{eff}\left(x - L_g - d_D\right)^2/\varepsilon_{si} \quad (7)$$

$$\phi_{R2}(x) = \phi_L + \frac{(\phi_{R1}(0) - \phi_L)sinh\left((L_g - x)/\lambda\right) + (\phi_{R3}(L_g) - \phi_L)sinh(x/\lambda)}{sinh(L_g/\lambda)} \quad (8)$$

When the depth ($d$) of the shell doping ($N_d$) is equal to half of the film thickness ($T_{si}/2$), then CS JL device behaves as a conventional JL MOSFET [7], i.e. without any core (undoped) region. The modeled results (represented by solid lines) in Figs. 2 and 3 are validated with Atlas simulation [9] results (represented by symbols). As shown in Fig. 2*a*, a lesser number of available dopants for narrow $d$ allows easy penetration of gate electric field into Source/Drain (S/D) region, resulting in a longer S/D extension length ($d_S$ and $d_D$, respectively) for $d$ = 1 nm than $d$ = 5 nm. For a positive drain bias ($V_{ds}$ = 0.5 V), $d_D > d_S$. Fig. 2*a-c* shows that an improved gate control over the channel potential for shallower shell depth is due to the lower potential and electron concentration, and longer S/D extensions beyond the gate edges. The variations of potential obtained from the model along $x$- and $y$- directions agree well with the simulated data. The drain current ($I_{ds}$)–gate bias ($V_{gs}$) characteristics, shown in Fig. 2*d* by lines, are obtained from the modeled channel potential using the drift-diffusion approach of [8].

$I_{ds}$–$V_{gs}$ characteristics have been used to extract $V_{th}$ as the gate bias corresponding to a constant current level [10], and scaling limits through the estimation of Drain Induced Barrier Lowering (DIBL), $V_{th}$ roll-off and $S$ [7]. The developed model results (solid line) in Fig. 3*a-h* agree well with simulated data (symbol). The performance of CS JL device improves at shallower shell depths as shown by relatively lower DIBL and $S$ values for gate length ($L_g$) of 15 nm in Fig. 3*a*, while achieving acceptable positive values for $V_{th}$ (Fig. 3*b*) for $d < 0.6(T_{si}/2)$. For CS JL device ($d$ = 3 nm), positive $V_{th}$ values (Fig. 3*c*) are achieved at lower gate workfunction ($\varphi_g$) as compared to conventional JL ($d = T_{si}/2$) MOSFETs. $V_{th}$ sensitivity is estimated by the rate of change of $V_{th}$ with respect to $T_{si}$, i.e. $dV_{th}/dT_{si}$ and is represented by $m_1$ and $m_2$ for CS JL and conventional JL MOSFETs, respectively, in Fig. 3*d*. Also, the net change in $V_{th}$ across the desired range of $N_d$ and $L_g$ is shown in Fig. 3*e–f*. Lower $V_{th}$ sensitivity values of around -20 mV/nm (@ $T_{si}$), 30 mV (@ $N_d$) and 40 mV (@ $L_g$) are observed for CS JL MOSFET ($d$ = 3 nm) in comparison to -100 mV/nm (@ $T_{si}$), 90 mV (@ $N_d$) and 60 mV (@ $L_g$) for conventional JL device [7] for varying $T_{si}$ (Fig. 3*d*), $N_d$ (Fig. 3*e*) and $L_g$ (Fig. 3*f*), respectively. The notable reduction from -100 mV/nm to -20 mV/nm indicates the much reduced sensitivity towards film thickness in CS JL MOSFET. $V_{th}$ roll-off of 40 mV (Fig. 3*f*) in CS JL device makes it more scalable than conventional JL MOSFET. A CS JL device with a narrow $d$ may impose stringent fabrication requirements, whereas a wider $d$ may display features similar to a conventional JL device. Therefore, optimization of $d$ and $T_{si}$ is essential. Fig. 3*g-h* showcases the design flexibility offered by shell doping to achieve $V_{th}$ values between 0.2 V and 0.3 V for different pairs of $d$ and $T_{si}$. For a moderate shell doping ($5\times10^{18}$ cm$^{-3}$), it is advantageous to select thicker film thickness (14 nm - 15 nm) and $d$ varying from 5 nm to 6.5 nm (in Fig. 3*g*) to achieve $V_{th}$ between 0.2 V and 0.3 V. If a higher shell doping ($10^{19}$ cm$^{-3}$) is selected (in Fig. 3*h*), then $d$ = 4 nm allows a broad range of $T_{si}$ (10 nm to 13 nm) to achieve the same $V_{th}$ range. Also, for $d$ = 3.7 nm, the flexibility in $T_{si}$ values (11 nm to 15 nm) can also be exploited to achieve the desired $V_{th}$ range. In an optimal design, shell depth (being a process parameter) should be fixed to ascertain the $T_{si}$ range for the desired $V_{th}$.

## 3. Conclusions

The semi-analytical modeling approach, through appro-

priate boundary and continuity conditions across the three regions, has facilitated the estimation of scalability and $V_{th}$ sensitivity in CS JL MOSFETs, which are in reasonable agreement with TCAD simulations. The developed model allows the determination of various $d$ and $T_{si}$ combinations to tune $V_{th}$ to desired levels while maintaining optimal device performance in the sub-20 nm gate length regime.


## Acknowledgements

This publication is an outcome of the R&D work undertaken in the project under the Visvesvaraya Ph.D. Scheme of Ministry of Electronics & Information Technology, Government of India, being implemented by Digital India Corporation.


## References


[1] Y.-J. Lee *et al., IEEE IEDM Tech. Dig.* (2014) 32.7.1.
[2] Y.-J. Lee *et al., IEEE IEDM Tech. Dig.* (2015) 6.2.1.
[3] M. P. V. Kumar *et al.,* IEEE Trans. Elect. Dev. **62** (2015) 3541.
[4] Y. V. Bhuvaneshwari *et al.,* Semi. Sci. Tech. **33** (2018) 115020.
[5] M. H. R. Ansari *et al.,* IEEE Trans. Elect. Dev. **66** (2019) 428.
[6] K. K. Young, IEEE Trans. Elect. Dev. **36** (1989) 399.
[7] N. Jaiswal *et al.,* IEEE Trans. Elect. Dev. **65** (2018) 881.
[8] A. Gnudi *et al.,* IEEE Trans. Elect. Dev. **60** (2013) 1342.
[9] ATLAS User's Manual, Silvaco Inc. (2015).
[10] S.-J. Choi *et al.,* IEEE Trans. Elect. Dev. **32** (2011) 125.


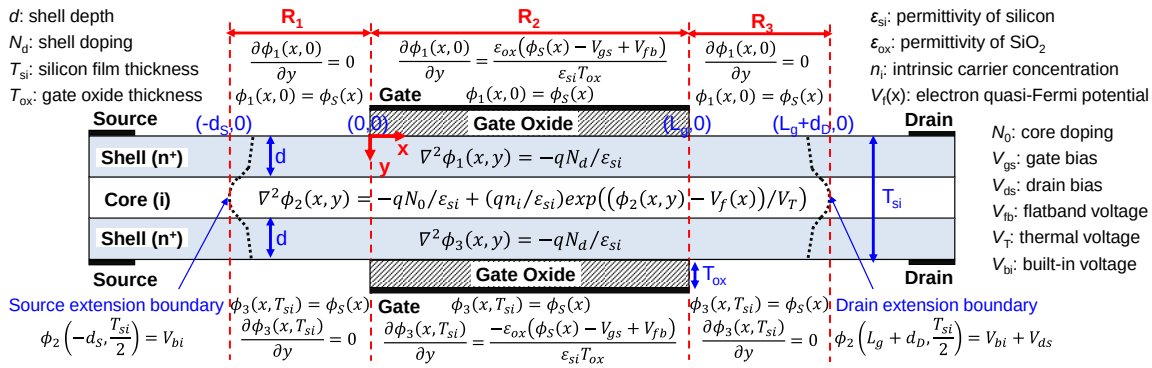


Fig. 1 Schematic representation of a Core-Shell (CS) JL MOSFET showing heavily doped shell (near the surface) and undoped (central) core regions. The gated region ($R_2$) has a gate length $L_g$, whereas the ungated source ($R_1$) and drain ($R_3$) regions, as defined by S/D extension boundaries, are of (S/D extension) lengths $d_S$ and $d_D$, respectively. The distinct boundary conditions are marked corresponding to each region. The potentials and their first order derivatives are continuous across regions along both $x$- and $y$- directions.

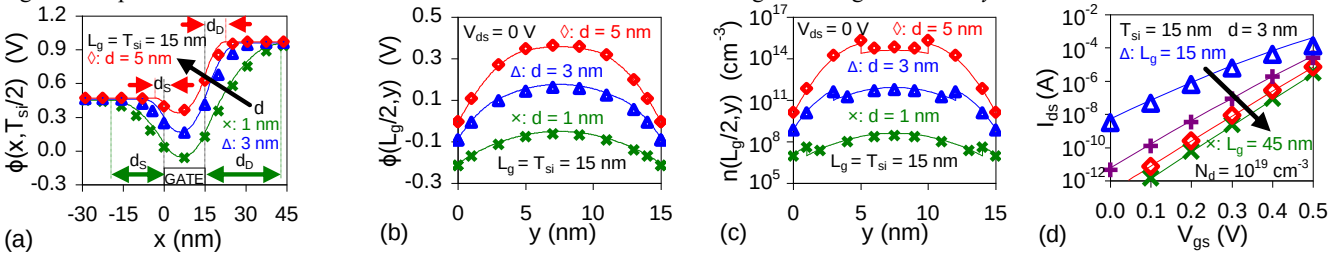


Fig. 2 Variation of channel potential at $V_{gs}$ = 0 V (a) along $x$-direction at centre of silicon film and (b) along $y$-direction at mid-gate position, and (c) electron concentration along $y$-direction at mid-gate position for $d$ = 1 nm, 3 nm and 5 nm. (d) Drain current-gate bias characteristics for $d$ = 3 nm with $L_g$ varying from 15 nm to 45 nm at steps of 10 nm at $V_{ds}$ = 0.5 V. Other parameters: $T_{ox}$ = 1 nm, $N_d = 10^{19}$ $cm^{-3}$ and $\varphi_g$ = 5.1 V. Solid lines: model results; symbols: simulation data.

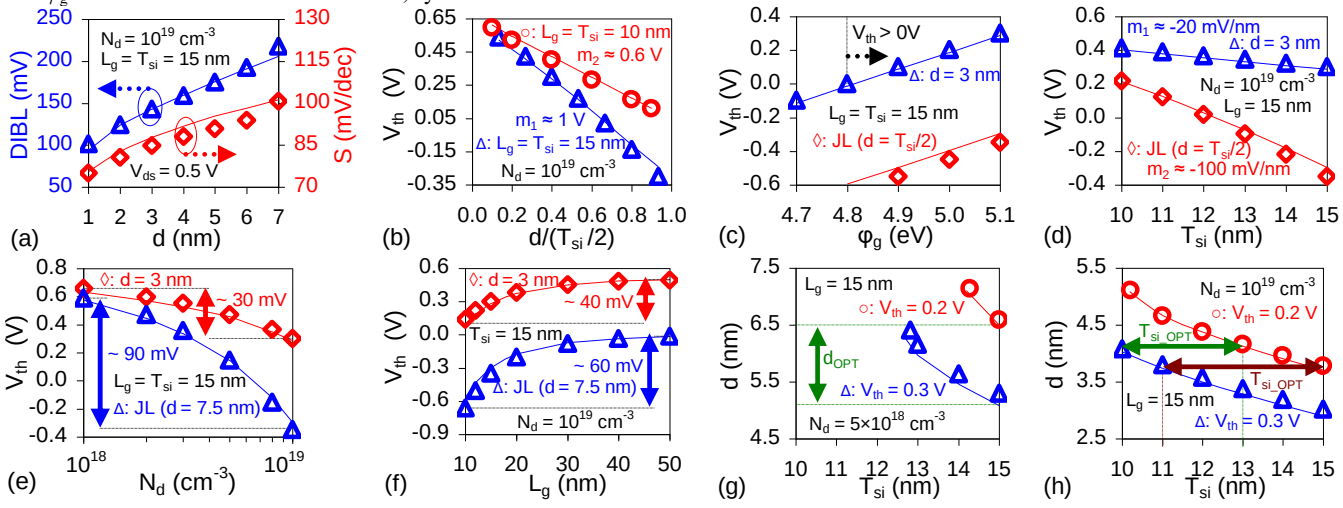


Fig. 3 Dependence of (a) DIBL and $S$, and (b) $V_{th}$ on $d$ and $T_{si}$. Plot of $V_{th}$ versus (c) $\varphi_g$ (d) $T_{si}$ (e) $N_d$ and (f) $L_g$ for CS JL ($d$ = 3 nm) and conventional JL ($d = T_{si}/2$) devices. Model results for conventional JL are obtained using [7]. The notation $m$ in Fig. 3*b,d* denotes slope of the respective curves. Design window offered by CS JL MOSFET to achieve $V_{th}$ of 0.2 V and 0.3 V for (g) $N_d = 5\times10^{18}$ $cm^{-3}$ and (h) $N_d = 10^{19}$ $cm^{-3}$. $d_{OPT}$ and $T_{si\ OPT}$ represent the optimal range of $d$ and $T_{si}$, respectively. Solid lines: model results; symbols: simulation data.