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Impact of Hafnium Oxide-Based Ferroelectric Material on Monolayer Black Phosphorus Transistor for Negative Capacitance and Memory Application

K.-T. Chen[1, 2], Y.-F. Chung[1], Y.-T. Tang[3]. S. T. Chang[1,*] and M. H. Lee[2,**]

[1] Department of Electrical Engineering, National Chung Hsing University, Taichung, Taiwan
[2] Institute of Electro-Optical Science and Technology, National Taiwan Normal University, Taipei, Taiwan
[3]Taiwan Semiconductor Research Institute, Hsinchu, Taiwan.
[*]E-mail: stchang@dragon.nchu.edu.tw [**]E-mail: mhlee@ntnu.edu.tw

Abstract

In this work, a compact band model for monolayer black phosphorus (BP) is proposed and integrates with hafnium oxide-based ferroelectric material for negative capacitance (NC) and memory application. For NC effect, TCAD simulation result shows monolayer BP NC-FET with HZO ($HfZrO_x$) has better subthreshold swing (SS). For memory application, TCAD simulation also shows that monolayer BP Fe-FET with silicon doped HfO_2 (Si:HfO_2) has good memory window (MW).

1. Introduction

Hafnium oxide based CMOS compatible ferroelectric materials such as Zr or Si doped in HfO_2 as gate stack has been intensively and extensively investigated to integrate with FETs due to following current CMOS architectures and feasibility ALD (atomic layer deposition) supercycle approach [1-2]. Recently, nearly equal mixture of ZrO_2 and HfO_2 and annealing for ferroelectric transition demonstrate negative capacitance field effect transistor with steep-slope (NC-FET) [3]. Dr. T. Ali's TED paper reported the integration of a ferroelectric (FE) silicon-doped hafnium oxide material in ferroelectric field effect transistor (FeFET) devices fabricated with an optimized interfacial layer in a gate-first scheme and the FE Si:HfO_2-integrated FeFET devices show a low-power operation capability as well as an improved endurance characteristics without jeopardizing high-temperature retention [4]. Two-dimensional materials such as monolayer black phosphorus owing to the unique electronic properties of the atomically thin two-dimensional layered structure can be made into the future metal–oxide–semiconductor field-effect device technology. In this work, ferroelectric HZO ($HfZrO_x$) applied on monolayer black phosphorus (BP) NC-FET is investigated by TCAD simulation and demonstrated with improvement on subthreshold swing (SS) to overcome the physical limitation A ferroelectric Si doped HfO_2 (Si:HfO_2) FeFET has been integrated into a 22nm FDSOI CMOS platform [5] and ferroelectric HSO (Si:HfO_2) applied on monolayer BP Fe-FET is also explored by TCAD simulation in this study.

2. Simulation Methodology

We propose compact band model for monolayer BP considering up to the high order non-parabolic correction [6]. Carrier mobility calculation to use Kubo–Greenwood Mobility formula is employed in this work [7] for electron mobility calculation of monolayer BP. The physical models in TCAD simulation are carefully calibrated with the dissipative quantum transport model using NEGF formalism in [8]. The dynamic of FE polarisation can be described by the Landau–Khalatnikov (LK) equation [9] for NC-FET simulation. A new simple and analytical polarization–electric field (P–E) relation for the ferroelectric material is proposed, including the unsaturated polarization and we used it in Fe-FET simulation [10].

3. Results and discussion

We consider a ferroelectric device with a FE layer, hafnium oxide interfacial layer (IL) and 20 nm thickness buried oxide in substrate as shown in Fig. 1. With the physical properties judiciously chosen from the published experimental and theoretical literature [5-7], TCAD simulations are performed to evaluate monolayer BP NC-FET and Fe-FET. The drain current I_{DS} versus V_{GS} characteristic of monolayer BP FET is presented in Fig. 2. Calibrated with the dissipative quantum transport model using non-equilibrium Green's function formalism in [8]. From the figure, we can clearly see that our simulation is in agreement with the result in [8]. The structure of the monolayer BP NC-FET is designed to have a channel length (L_g) 15 nm as shown in Fig. 1. TCAD simulation for monolayer BP NC-FET will consider various physical models as mentioned in [11]. The FE material is 10 nm HZO which could be simulated by the Landau–Khalatnikov (LK) model. The parameters are used in this work to fit the experimentally measured P-V data (polarization-voltage) of metal/FE-HZO/metal as shown in Fig. 3. Fig. 4 shows the I_{DS}-V_{GS} transfer characteristics and SS as a function of drain current of monolayer BP FET and NC-FETs with different FE thicknesses. As NC effect is considered, the I_D-V_G transfer characteristic curve is pulled to the small voltage region overall, so it can reduce both threshold voltage and subthreshold swing. It brings out monolayer BP NC-FET to achieve low voltage steep slope transistors in the development of sub-5nm technology. The key features of these simulations is using silicon doped hafnium oxide (Si:HfO_2) as a ferroelectric layer. Four transistor geometrics were created, the first one has 15 nm, the second one has 12 nm, the third one has 10 nm, and the last one has 8 nm of Si:HfO_2 as a ferroelectric layer. All these devices have 8 Å of HfO_2 as a buffer layer. The main purpose of simulating devices with different ferroelectric thicknesses was to study the effect of the ferroelectric thickness on the performance of the FeFET. The gate voltage was swept from -3.5 V to +3.5 V for all FeFET devices. Then, the sweep amplitude was decreased to 0 V while keeping the drain voltage at 0.1 V. Fig. 5 shows the simulated the I-V hysteresis loops for monolayer BP FeFETs. Since the remnant polarization of Si:HfO_2 considerably increased by decreasing the layer thickness, the memory window (MW) decreased. The advantage of using thinner layer of Si:HfO_2 ferroelectric material is the possibility of accom-

plishing ultra low-power FeFET memory devices. As seen in Fig. 5, the Memory window (MW) decreased from 1.47 V to about 0.96 V as the ferroelectric layer thickness was decreased from 15 nm to 8 nm, respectively.

4. Conclusion

In this study, compact band model is proposed for band structure and electron mobility calculations of monolayer BP. Impact of the HfO_2-based FE materials on monolayer BP transistors are also discussed. This work will help the design of future nanoscale transistor device and memory using monolayer BP and HfO_2-based FE materials.

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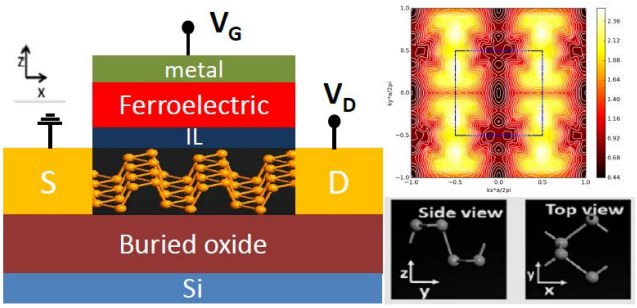

Fig. 1 The ferroelectric transistor based on monolayer black phosphorus. Sketch of the simulated monolayer BP NC-FET/Fe-FET. The SiO_2/Si substrate is beneath the 2D monolayer BP channel. Transport direction is assumed to be the armchair direction of monolayer BP. Constant energy contour of conduction band for monolayer BP from first principle calculation is also included for information. Monolayer BP unit-cell is in the inset. We assume ideal doped contacts with aligned conduction band for the monolayer BP n-type ferroelectric transistor device.

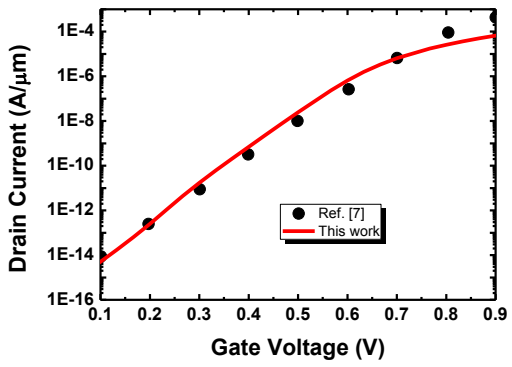

Fig. 2 I_{DS}–V_{GS} characteristics of monolayer BP FET at V_{DS} = V_{DD}. Our calibration with the data in Ref. [7].

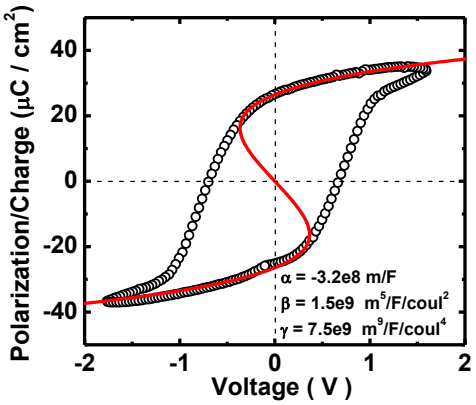

Fig. 3 Experimental measurement of P-V hysteresis loop for the M/FE-HZO/M structure, and the red curve models the NC using the Landau–Khalatnikov (LK) model.

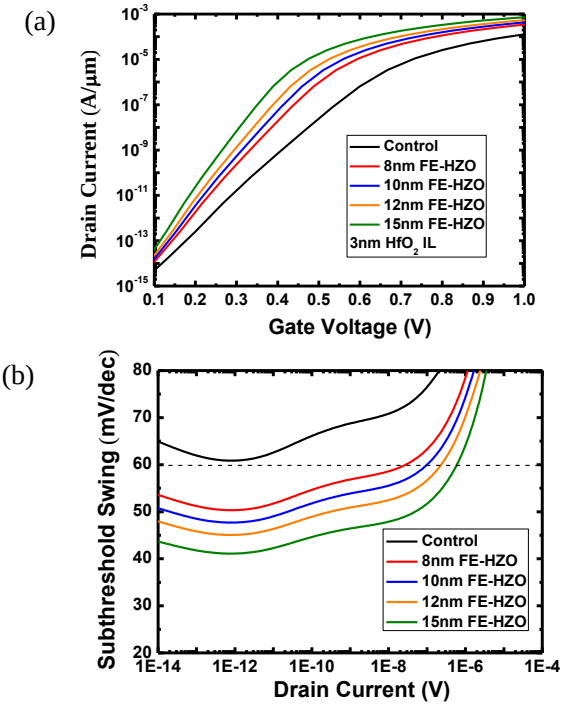

Fig. 4 (a) I_{DS}–V_{GS} for 15 nm channel length and 3 nm HfO_2 insulator layer monolayer BP FET (control) and NC-FETs with different ferroelectric layer thicknesses (FE-HZO) at V_{DS}=0.5 V and T=300 K. (b) SS as a function of drain current of 15 nm monolayer BP FETs and monolayer BP NC-FETs with different ferroelectric layer thicknesses at V_{DS}=0.5 V and T=300 K.

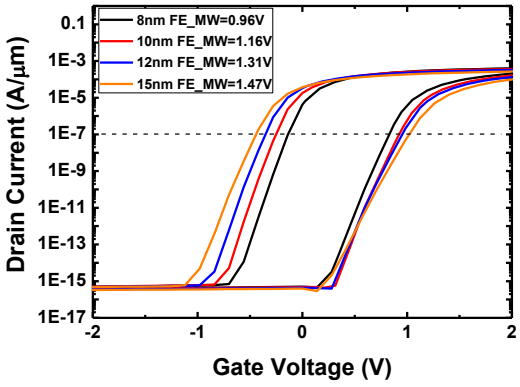

Fig. 5 Effect of ferroelectric layer thickness on memory window (MW) of monolayer BP FeFET with 0.8 nm HfO_2 IL.