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# Memory window and retention time of double back gate Z²-FET

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**Abstract**

**The electrical characteristics of Z²-FET has been controlled by double back gates. Comparing with the Z²-FET with a single back gate, memory window is increased by 0.2V and retention time becomes much longer from 60μs to 5ms by applying negative bias to the p-type back gate under the same bias conditions of front gate and drain. The improved performance is explained with the band modulation effect of double back gates.**

## 1. Introduction

Capacitor-less single transistor type memory (1T-DRAM) has been a desperate demand for resolving scaling limit and high fabrication cost due to capacitor in the conventional DRAM structure As a candidate cell device, Z²-FET (Zero impact ionization, zero subthreshold swing) has been proposed since it shows steep swing slope and low turn on voltage [1-2]. However, Z²-FET is still not only fully understood, but, first of all, it also needs to improve memory window and short retention time of '0' state, which are the most important issues for ensuring the memory operation [3-4]. In this work, we have suggested a new device structure by dividing the back gate into n and p-type gates and controlling the bias of each back gate differently to improve these two issues. To explain effects of double back gates and relationships among the carrier injection barriers, the memory window, and retention time, we have done TCAD simulation of energy band modulation in the channel region.

## 2. Experiments

The single and double back gate structures of Z²-FET are fabricated on p-type Si substrate ($N_{Sub} \approx 10^{18}$ cm$^{-3}$) by using 28nm fully depleted silicon on insulator (FDSOI) technology as shown in Fig. 1. The SOI body is doped with B ($N_{SOI}=10^{16}$ cm$^{-3}$), and highly doped Boron drain and Arsenic source regions ($N_{D/A} > 10^{20}$ cm$^{-3}$). The thickness of the intrinsic SOI body under the front gate ($t_{si}$) is 7nm and the buried oxide ($t_{BOX}$) laying above the back gate is 25nm. The front gate insulator ($t_{fox}$) composed of $SiO_2$/HfON multilayer is 1.5nm. The total length is 200nm, which is divided into the front gate ($L_G$) and the ungated region ($L_{IN}$). The double back gates are separated with the n-type back gate (GbN) at the just opposite side of the $L_G$ and the p-type back gate (GbP) is located at the $L_{IN}$ side.

## 3. Results and Discussions

*A. Memory window*

The memory windows of single and double gate devices are measured with increasing the drain (read) voltage at the same front gate voltage ($V_{Gf}$) of 1.2 V for determining the proper range of memory operation. The back gate voltage ($V_{Gb}$) is fixed at -1.0V for the single gate, and for the double back gates -1.0 V is also applied separately to the GbN ($V_{GbN}$) and GbP ($V_{GbP}$). As a result, both '0' and '1' state is written and read with increased read voltage and the turn on voltage of each state and the current during the read process are shown in Fig. 2. Interestingly, when $V_{GbP}$ is applied to GbP, the memory window represented by red line is larger than the case of that $V_{GbN}$ is applied to GbN by 0.2V. And, the memory window of the single back gate device is the same as the latter. This means that the bias of the p-type back gate enhances larger memory window comparing the whole covered back gate and n-type back gate. From the TCAD simulation of energy band diagram for the single back gate device, the negative biasing on the whole back gate lowers the hole injection barrier height in the drain junction, which reduces the memory window [5]. However, when the negative bias is applied only to the GbP located at the ungated side, the hole and electron injection barriers on the both junctions are not reduced by the $V_{GbP}$.

*B. Retention time*

In Z²-FET, normally, '1' state is maintained very long to provide readable differential voltage for the sense amplifier. But, the '0' state is microsecond order and quickly failed with high current. The shorter retention time of '0' state is explained with several factors such as Shockley-Read-Hall (SRH) generation and band to band tunneling [6]. Therefore, we have thought that the key point is to prevent the collapse of injection barriers by controlling $V_{GbN}$ and $V_{GbP}$ separately. Particularly, according to our previous work [5], it is found that when the back gate bias is applied to the whole SOI body, the changes in the energy barrier on the $L_{IN}$ become relatively bigger than that of the $L_G$ region where the electric field will be reduced by $V_{Gf}$. The retention time of both '0 and '1' states for the single and double back gate Z2-FET is measured with write – read – hold – read (W-R-H-R) sequences. First, '0' or '1' state is written and then, read to verify the state and after a certain hold time, we read again to determine the holding time. Under the hold condition, the $V_{Gf}$ is biased positively and $V_D$ is not biased. In Fig. 3, '0' state was written by W0

voltage represented by black line and low current represented by blue line was detected by the read voltage (R). As a result, the retention time of single back gate device is 60μs as shown in Fig. 3 (a). However, the double back gate devices show much improved retention time. When $V_{GbN}$ is applied to GbN, the time is 1ms and for the case of GbP it is increased up to 5ms. This result is quite well agreed with our expectation that the energy barrier lowering on the $L_{IN}$ side could be prevented by applying the negative bias to GbP. We will discuss the TCAD simulations of each case with experimental results in detail. In Fig. 4, the retention time and current margin of the double back gate device are measured with various drain voltage. Increasing the drain (read) voltage, the retention time decreases in reverse. In other word, this figure suggests that the retention time could be increased by decreasing the read voltage when negative bias is applied to GbP. The reason is that if $V_D$ is slightly decreased and the GbN is grounded, the hole carriers injection barrier is not significantly reduced and the electron barrier on the source junction will be relatively higher than the hole barrier by the negative $V_{GbP}$, which resulting in that '0' state is maintained due to low carrier injections at the both junctions. Thus, the retention time of '0 state is quite well prolonged by controlling the electron injection barrier. However, in this case, the current margin seems to be reduced, where a tradeoff point is between the retention time and current margin. These results suggest that if we can scale down of double back gate $Z^2$-FET, the $V_D$ will be below 1.0V and the longer retention time and lower power consumption could be ensured.

## 4. Conclusions

We have suggested a double back gate structure for improving the memory window and retention time of $Z^2$-FET. Experimental results and TCAD simulations reveal that memory window is increased by 0.2 V, and the retention time of '0' state is significantly prolonged from 60μs to 5ms when the negative bias is applied to the p-type half back gate on the $L_{IN}$ side. These improvements are ascribed to the modulation of energy barrier on the $L_{IN}$ side.


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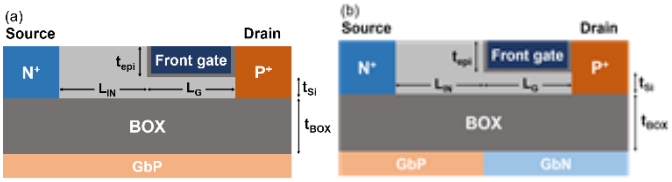


Fig.1 Schematic diagrams of (a) single back gate $Z^2$-FET and (b) double back gate $Z^2$-FET. GbP stands for p-type back gate and GbN stands for n-type back gate.

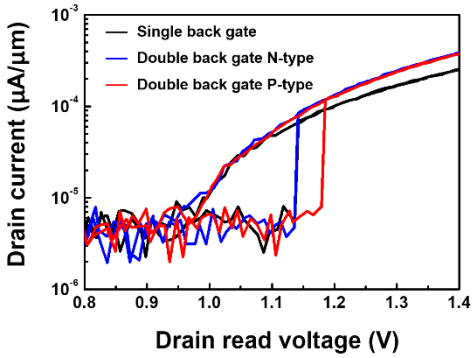


Fig.2 Memory window of the single back gate (black) and double back gate $Z^2$-FETs (blue and red).

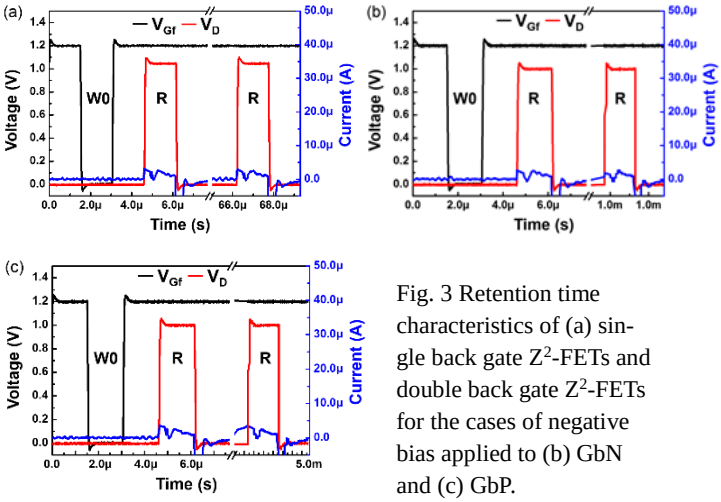


Fig. 3 Retention time characteristics of (a) single back gate $Z^2$-FETs and double back gate $Z^2$-FETs for the cases of negative bias applied to (b) GbN and (c) GbP.

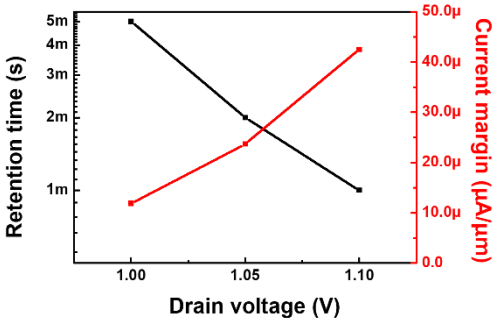


Fig. 4 Retention time and current margin vs drain (read) voltage at $V_{GbP}$=-1V.