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Extremely low temperature selective epitaxial processes for advanced CMOS applications

Andriy Hikavyy, Clement Porret, Erik Rosseel, Paola Favia, Roger Loo

imec
Kapeldreef 75
Leuven 3001, Belgium
Phone: +32 16 28 1120, E-mail: Andriy.Hikavyy@imec.be

Abstract

Selective epitaxial growth of SiGe:B and SiGe:P layers at a very low growth temperature of 400ºC in a commercial RPCVD epi tool is presented. The process was verified on device wafers to confirm their compatibility with advanced processes. A fine multilayered structure of the deposited layers reflecting the cyclic nature of the processes has been observed. High active concentrations of ~ $6e^{20}$ cm^{-3} and ~ $1e^{20}$ cm^{-3} for B and P are obtained, suitable for low temperature Source/Drain application of novel advanced device structures.

1. Introduction

One of the most obvious trends in group IV epitaxy is a systematic lowering of process temperature. This is governed by few reasons. On one hand novel device concepts which must fulfill scaling paradigm like gate all around FETs [1], complementary FETs [2], 3D stacked devices [3], etc. put stringent temperature requirements to epitaxy due to complex geometry and application of new approaches (complex high-k materials, buried power rail, etc.). On the other hand introduction of SiGe and Ge in the device's channel or SiGe with high Ge content, Ge, GeSn, SiGe:Sn as source/drain (S/D) materials requires rather dramatic decrease of the epi process temperature in order to maintain layers properties.

In view of this trend use of high order Si and Ge precursors allowing development of epi processes at temperatures well below 500ºC becomes very promising [4]. Combining such processes with Cl_2 which allows etching down to extremely low temperatures of ~ 400ºC in the case of Si and ~250ºC for Ge [5] open possibilities for development of selective SiGe processes at temperatures of 400ºC and below. A visibility of such selective cyclic SiGe:B and SiGe:P at 400ºC has been demonstrated on Shallow Trench Isolation (STI) wafers in [6].

In this work we elaborate further on integration of these processes in CMOS flow when full device comprising spacers, metal gates and hard masks is built. Morphological, electrical and structural properties are presented as well.

2. Experimental details

Epitaxial growth reported here was done on patterned wafers in the frame of 3D sequential stacked planar devices work with a typical processing flow reported in [3] using an ASM Intrepid XP™ epi tool, which is a horizontal cold wall, load-locked reduced pressure chemical vapor deposition system designed for production applications.

Low temperature selective growth of SiGe layers was done using high order precursors: disilane (Si_2H_6) and digermane (Ge_2H_6) as Si and Ge precursors. B_2H_6 (B_2H_6 1% in H_2) or PH_3 (PH_3 15% in H_2) and Cl_2 were used as p and n type dopants and etching gases respectively. Peculiarities of the growth and selectivity tuning has been reported elsewhere [6].

A micro four-point-probe using the CIPTechTM M300 Micro Hall system from Capres A/S was used in order to measure active carrier concentration [7]. Scanning electron microscopy (SEM) was performed on EXPIDA1285 from FEI and eDR-7100 from KLA Tencor. Transmission electron microscopy (TEM) and high angle annular dark field scanning transmission electron microscopy (HAADF-STEM) was studied in Tecnai 30 F microscope operating at 300 kV.

3. Results and discussion

An application of the SiGe:B low temperature process developed in [6] to a device wafer for 3D stack integration resulted in a severe selectivity loss. It is well known that selectivity of a process depends on the type of oxides and nitrides used and usually must be tuned for each specific application.

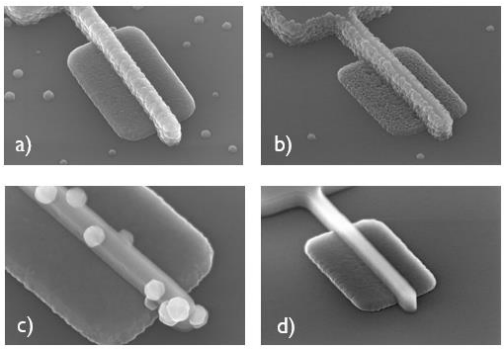

Fig. 1. Selectivity tuning of cyclic SiGe:B : long deposition/short etch a), long deposition/long etch b), short deposition/short etch c), final tuned selective process d).

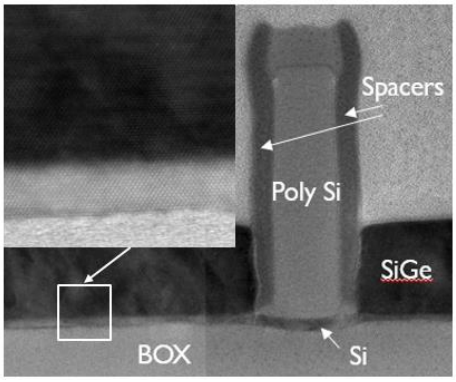

Fig. 2. Selective low temperature cyclic SiGe:B grown in S/D areas of a planar device wafer for 3D stack integration. SiGe was grown on an SOI wafer with Si thickness of 5 nm.

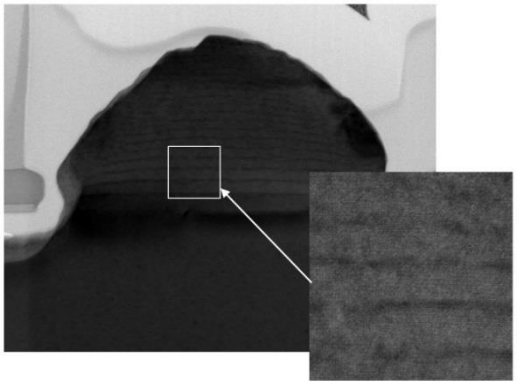

Fig. 3. Selective low temperature cyclic SiGe:P grown on relaxed Ge in the patterned wafer for Circular Transmission Line Measurement.

Since in our case we apply a cyclic process, the main tuning knob to recover selectivity is etch/deposition times. Fig. 1 presents results of four different cases: long deposition/short etch (a), long deposition/long etch, short deposition/short etch (c) and final tuned selective process.

Careful optimization of both deposition and etching allows to obtain a process which is selective to both oxides (Shallow Trench Isolation and hard masks on top of gates) and nitrides (spacers).

A cyclic nature of the process can be directly seen in transmission electron microscopy (TEM). Although Energy Dispersive X-Ray Spectroscopy (EDS) showed uniform over the layer thickness Ge concentration of ~ 40%, both high resolution TEM and high-angle annular dark-field imaging (HAADF) show that S/D consists of a number of SiGe layers which are separated with few atomic layers of SiGe with a darker contrast suggesting presence of SiGe with lower Ge concentration. These intermediate low Ge concentration layers are formed after an etching step and can be explained by Cl_2 preferential Ge pull out of the SiGe surface. Despite of this peculiarity SiGe:B layers demonstrated very good quality and high active B concentration of ~ $6e^{20}cm^{-3}$ which is suitable for Si-based pMOS S/D application.

In the case of Ge-based devices selective SiGe:P is an interesting option for the n-MOS S/D since it typically offers higher active P concentration compared to selective Ge:P and tensile stress to the channel. In frame of this work we evaluated a similar growth strategy for SiGe:P. The selectivity tuning strategy was similar to SiGe:B (Fig.1) and described in [6]. A TEM image of the final SiGe:P layer with Ge concentration ~ 75% is shown in Fig. 3. A multi structure of SiGe:P similar to Fig.2 reflecting the process cyclic nature has been observed. Blanket experiments of the deposition part of this process showed that active P concentration of ~ $1e^{20}$ cm^{-3} can be achieved when both Ge and P flows are optimized.

4. Conclusions

In this work we investigated selective growth of SiGe:B and SiGe:P at temperature of 400°C to be used in advanced device structures. Careful optimization of both deposition and etching allows to obtain processes which are selective to both oxides and nitrides present on the device wafers. A fine multilayered structure of the deposited layers is explained by the cyclic nature of the processes and Ge pull out effect during Cl_2 etching step. High active concentrations of ~ $6e^{20}$ cm^{-3} and ~ $1e^{20}$ cm^{-3} for B and P suitable for low temperature Source/Drain application of novel advanced device structures are obtained.

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