Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp965-966

Enhanced Electrical Performance and Reliability of Ti-IGZO Thin-Film Transistors with $Hf_xAl_{1-x}O$ Gate Dielectrics

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Abstract:

In this work, thin-film transistor (TFT) with Ti-IGZO channel layer and $Hf_xAl_{1-x}O$ gate dielectric is proposed to improve device performances and reliability. Experimental results reveal that, among three types of HfO_2/IGZO, $Hf_{1-x}Al_xO$/IGZO, and $Hf_{1-x}Al_xO$/Ti-IGZO based TFTs, the $Hf_{0.88}Al_{0.12}O$/Ti(2.0%)-IGZO TFT could exhibit the best device performances with the subthreshold swing of 86 mV/dec, field effect mobility of 28.63 $cm^2/V{\cdot}s$, on/off current ratio of 3.26×10^8. Especially, it shows a hysteresis voltage as low as 0.02 V and a threshold voltage shift after 1000s positive/negative gate bias stress/white light illumination of 0.134 V/-0.089 V/-0.195 V, and as compared with the HfO_2/IGZO TFT which has corresponding values of 0.48 V and 0.612 V/-0.507 V/-0.781 V. The remarkable improvements are attributed to the Al incorporation could reduce oxygen vacancies and improve surface roughness of HfO_2 to suppress surface scattering and the amount of charge trapping during the stress test as well as Ti incorporation reduces defect density in the channel layer.

1. Introduction

α-IGZO TFT with advanced performance and superior stability is highly desired for applications of active-matrix flat-panel display applications (AMFPDs). Nevertheless, owing to interstitial zinc atoms and oxygen vacancies from weak In-O bonds in α-IGZO channel, α-IGZO TFTs usually encounter reliability issue caused by charge trapping via internal or external defect states [1]. Instability in electrical characteristics of TFTs might result in incorrect gray scales and poor screen performance. Continuing improving the qualities of the gate dielectric and the channel layer system is very crucial to meet the urged demands of better image quality and reliability.

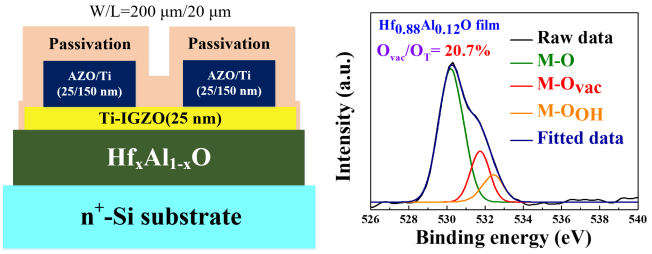
To enhance gate controllability, reduce leakage current and operation voltage, the use of appropriate high-κ dielectrics to replace currently used Si_3N_4/SiO_x is urgently required. Over the past few decades HfO_2 having a high-dielectric constant (~25) is one of the most promising high-κ materials. However, binary HfO_2 suffer from high defect density and low poly-crystallization temperature, which could impair device performance and stability [2]. To tackle this issue, incorporation of Al_2O_3 into HfO_2 to form ternary an $Hf_xAl_{1-x}O$ gate dielectric and incorporation of Ti into IGZO channel are proposed in this work. The former which could reduce oxygen vacancy and increase the crystallization temperature to suppress surface scattering and interface trap density is expected to strengthen the breakdown field, improve thermal and chemical stability [3-5], because Al creates an acceptor-like level in HfO_2 and could interact with the surrounding oxygen to repair oxygen vacancies [6]. While the latter is to reduce defect density, for having a high binding energy with oxygen O1s (~458.5 eV) and high enthalpy of Ti-O (672 kJ/mol) [7]. Results of material analysis and characterization of $Hf_xAl_{1-x}O$ dielectric and Ti-IGZO prepared by a co-sputtering process are presented. Comparisons of device performances with emphasis on reliability between the TFTs with the proposed dielectric and channel materials and IGZO TFTs are made. Superior stability of the proposed TFTs under gate bias stress and white light illumination are reported and discussed.

2. Experimental

Fig. 1(a) depicts the schematic cross section view of the fabricated Ti-IGZO TFT with a bottom $Hf_xAl_{1-x}O$ gate dielectric. $Hf_xAl_{1-x}O$ gate dielectric layers with an equivalent thickness (EOT) of 9±1 nm were deposited on n^+-Si substrate using RF co-sputtering with HfO_2 and Al_2O_3 targets in Ar ambient at RT. To examine the influence of Al content on dielectric performance, various sputtering powers (0, 70, 80, and 90 W) were used for the Al_2O_3 target while that of the HfO_2 target was kept at 100 W. $Hf_{1-x}Al_xO$ layers with an x of 0, 0.08, 0.12, and 0.17, respectively were obtained from material analysis. It was then followed by a post-depositing annealing (PDA) at 600 °C for 10 min in O_2 ambient to improve material quality.

For device fabrication, a 25-nm-thick α-IGZO or Ti-IGZO channel layer was deposited on $Hf_xAl_{1-x}O$ dielectric films by RF sputtering using an IGZO (In_2O_3:Ga_2O_3:ZnO=1:1:1) target only or co-sputtering using an additional TiO_2 target. The sputtering power for IGZO was kept at 80 W and for TiO_2 at 20, 40, and 60 W, respectively, in Ar ambient at RT, which forms a Ti composition of 0.8, 2.0, and 2.7% in the Ti-IGZO channel layers. It was followed by a PDA at 300°C for 10 min in N_2 ambient to improve material quality. Subsequently, a patterned 25-nm-thick Al-doped ZnO (AZO) contact buffer layer and a 200-nm-thick Titanium (Ti) metal were deposited as the source/drain (S/D) electrodes by RF sputtering and e-beam evaporation, respectively. Finally, a 150-nm-thick SiO_2 was deposited as a passivation layer by RF sputtering. Note that all TFTs are with the same width/length ratio of 200 μm/20 μm.

To explore the effectiveness of Al incorporation in HfO_2 gate dielectric on TFT performance, two types of conventional α-IGZO TFTs with HfO_2 and $Hf_{0.88}Al_{0.12}O$ dielectric layers, namely device A and B, are investigated at first. Note that $Hf_{0.88}Al_{0.12}O$ layer was chosen for it shows the best dielectric and interfacial characteristics (to be discussed later). Finally, TFTs with a co-sputtering deposited Ti(2.0%)-IGZO channel with $Hf_{0.88}Al_{0.12}O$ dielectric layers, called device C, are prepared to clarify the effectiveness of Ti incorporation.



(a) (b)

Fig. 1 (a) Schematic of the Ti-IGZO TFTs with a $Hf_xAl_{1-x}O$ gate dielectric. (b) XPS of O 1s peaks for $Hf_{0.88}Al_{0.12}O$ film after PDA at 600 °C for 10 min in O_2 ambient.

3. Results and Discussion

Through C-V measurement, XPS, and Atomic Force Microscopy (AFM) analysis, κ-value, composition contents, and the surface roughness of $Hf_xAl_{1-x}O$ dielectrics are summarized in Table I. Based on experimental results, the κ-value and surface roughness of $Hf_xAl_{1-x}O$ dielectrics are about 27.9/22.7/21.3/19.1 and 0.893/0.165/0.153/0.172 for the sample prepared with 0/70/80/90 W sputtering powers for the Al_2O_3 target, respectively. It reveals that κ-value of the $Hf_xAl_{1-x}O$ dielectric decreases with increasing Al composition, which could be adjusted well by co-sputtering power ratio. Al-doped HfO_2 dielectrics exhibit a much lower surface roughness than that undoped one. Among these Al-doped HfO_2 dielectrics, note that $Hf_{0.88}Al_{0.12}O$ dielectrics (80 W for Al_2O_3 target) shows the lowest surface roughness, it could be attributed to the low surface roughness of the ternary oxide layer containing an appropriate ratio of aluminum [6].

Table I Al composition and dielectric constant of $Hf_xAl_{1-x}O$ films with different co-sputtering power ratios.

Power ratio: HfO_2(W):Al_2O_3 (W)	Al/(Al+Hf) (%)	Dielectric	κ	Roughness (nm)
100:0	0	HfO_2	27.9	0.893
100:70	8	$Hf_{0.92}Al_{0.08}O$	22.7	0.165
100:80	12	$Hf_{0.88}Al_{0.12}O$	21.3	0.153
100:90	17	$Hf_{0.83}Al_{0.17}O$	19.1	0.172

Based on XPS analyses (Fig. 1(b) for the 80 W case, others are not shown here for length limit of the paper), the O_{vac}/O_T area ratio are estimated to be of 29.1/24.1/20.7/25.3% for the 0/70/80/90 W sample, respectively, while the corresponding Al contents are of 0, 8, 12, and 17

%, respectively. It reveals that the amount of oxygen vacancies decreases with increasing Al composition in the range of 0-12% as expected. It is attributed to ionic radius of guest atom Al^{3+} (51 pm) is smaller than host atom Hf^{4+}(78 pm), which allows Al atom to dissolve into HfO_2 easily [8]. Al creates an acceptor-like level therein and interacts with the surrounding oxygen to repair oxygen vacancies [9]. Hence a considerable suppress in surface scattering and interface trap density after the channel layer deposition can be realized.

Fig. 2(a) shows the results of XRD analysis of HfO_2 and $Hf_xAl_{1-x}O$ films without and with PDA at 600 °C for 10 min in O_2 ambient. A considerable degree of amorphous-to-polycrystalline transition is evident after 600 °C thermal annealing for the HfO_2 layer, which would increase leakage current and deteriorate device performance. In contrast, the $Hf_xAl_{1-x}O$ layers remains amorphous structure even after 600 °C thermal annealing, it suggests that the incorporation of Al in HfO_2 layer could increase the transition temperature (T_c) at least up to 600 °C. As a result, a suppressed leakage current can be realized. Fig. 2(b) shows the J-V curve of MIM capacitors with HfO_2 or $Hf_xAl_{1-x}O$ dielectric film. A considerable decrease in leakage current is seen from the samples with Al incorporation due to the energy bandgap is enlarged and stable in the amorphous state. Note that the MIM capacitor with $Hf_{0.88}Al_{0.12}O$ dielectric shows the lowest leakage current among the prepared samples, conforming the superiority of the ternary oxide $Hf_xAl_{1-x}O$ film over the binary oxide HfO_2 films. Accordingly, $Hf_{0.88}Al_{0.12}O$ was chosen for devices fabrication in this study.

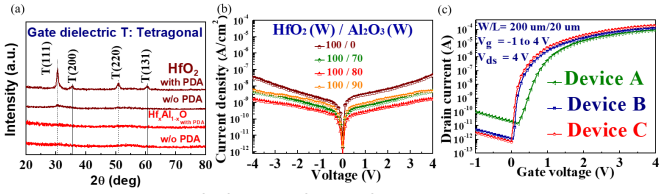


Fig. 2 (a) XRD analysis of HfO_2 and $Hf_xAl_{1-x}O$ films without and with PDA at 600 °C for 10 min in O_2 ambient. (b) J-V curve of MIM capacitors with HfO_2 and $Hf_xAl_{1-x}O$ dielectrics after PDA. (c) Transfer characteristics of the prepared TFTs.

Fig. 2(c) shows the transfer characteristics of the three types of TFTs (devices A, B, and C) prepared in this work. A comparison of device electrical parameters among our devices and the ones reported in the literature [10-11] are also listed in Table II. As is evident from the figure, as compared with device A, device B exhibits better electrical performance with an on/off current ratio (I_{on}/I_{off}) of 1.25×10^8, subthreshold swing (SS) of 93 mV/dec, and field-effect mobility (μ_{FE}) of 21.16 $cm^2/V\cdot s$, which suggests that the incorporation of Al in HfO_2 to form $Hf_{0.88}Al_{0.12}O$ could not only diminish oxygen vacancy but also reduce surface roughness to suppress the dielectric/channel interface trap density (D_{it}~1.17×10^{12} $cm^{-2}eV^{-1}$). Note that device C which is with $Hf_{0.88}Al_{0.12}O$ gate dielectric and Ti(2.0%) doped IGZO channel shows the best gate controllability with the highest I_{on}/I_{off} of 3.26×10^8, the lowest SS of 86 mV/dec, the highest μ_{FE} of 28.63 $cm^2/V\cdot s$, and the lowest D_{it} of 9.27×10^{11} $cm^{-2}eV^{-1}$, which reflects the effectiveness of Ti incorporation in IGZO channel in suppressing defect density especially at the dielectric/channel interface. TFTs with other Ti compositions (i.e., 0.8 and 2.7%) in the channel layer are not shown here for not exhibiting comparably better device performance than that of the device C.

Table II Electrical parameters of samples prepared in this study.

Device	I_{on}/I_{off}	V_{TH} (V)	SS (mV/dec)	μ_{FE} ($cm^2/V\cdot s$)	D_{it} ($cm^{-2}eV^{-1}$)
A	**5.23×10^6**	**0.67**	**138**	**12.87**	**2.97×10^{12}**
B	**1.25×10^8**	**0.25**	**93**	**21.16**	**1.17×10^{12}**
C	**3.26×10^8**	**0.20**	**86**	**28.63**	**9.27×10^{11}**
[10]	4.3×10^7	1.1	280	10.3(μ_{sat})	-
[11]	3.6×10^6	3.9	252	9.3	-

The hysteresis loops of the device A, B, and C under forward (-1 V to 4 V) and reverse (4 V to -1 V) sweeps are shown in Fig. 3 with a measured $\Delta V_{TH(hys)}$ of 0.48, 0.07, and 0.02 V, respectively. The difference in $\Delta V_{TH(hys)}$ can be explained by the degree of electron trapping in the dielectric/channel interface. It confirms again that the suitable incorporation of Al in HfO_2 dielectric and Ti in IGZO channel could not only reduce bulk defect density in the IGZO channel but also improve the quality of the dielectric/channel.

Fig. 4 shows the transfer characteristics of device C subjected to gate bias stress (GBS) at +4 V and -4 V and white light illumination (0.5 mW/cm^2) for 0, 10, 100, 1000 s. The threshold voltage shift (ΔV_{TH}) as a function of stress time for device A, B and C is shown in the inset of the figure. Note that the values of ΔV_{TH} after 1000s stress are listed and compared with those reported in the literature [12-13] in Table III. As compared with devices A, B, and reported data in [12-13], device C shows a significant improvement in device reliability with the ΔV_{TH} reduced from 0. 612V to 0.134 V (~78% reduction) after PGBS for 1000 s and from -0.507 V to -0.089 V (~82% reduction) after 1000 second NGBS, respectively. Such results agree very well with the transfer characteristics and hysteresis loops mentioned above.

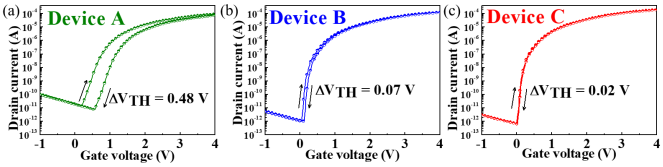


Fig. 3 Hysteresis loops of (a) device A (IGZO with PDA), (b) device B, and (c) device C under the forward (V_G = -1 to 4 V) and revers (V_G = 4 to -1 V) sweeps.

Upon white light illumination, photons-induced oxygen vacancies in IGZO and Ti-IGZO serve as shallow donor states to increase electron concentration which results in a negative ΔV_{TH}. As compared with device A, device B shows a significant improvement (~59% reduction) in ΔV_{TH} because $Hf_{0.88}Al_{0.12}O$ gate dielectric has a lower surface roughness and trap density. Device C shows a further reduction in ΔV_{TH} from -0.322 V to -0.195 V, corresponding to an additional reduction of ~39% in ΔV_{TH}, it also clarifies the benefit of Ti incorporation into the IGZO channel.

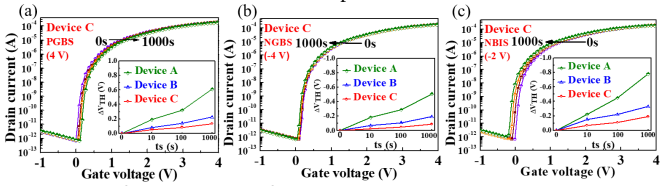


Fig. 4 The transfer characteristics of device C under gate bias stress and white light illumination. (a) PGBS, (b) NGBS, and (c)NBIS. The inset in these figure shows the measured ΔV_{TH} as a function of stress time for device A, B and C.

Table III ΔV_{TH} after PGBS and NGBS for 1000 s

ΔV_{TH} (V) (1000 s)	Device A	Device B	Device C	[12]	[13]
PGBS	0.612	0.225	0.134	-	-
NGBS	-0.507	-0.191	-0.089	~ -0.5	~ -1
NBIS	-0.781	-0.322	-0.195	~ -1	~ -2.5

Conclusions

Ti(2.0 %)-IGZO TFTs with $Hf_{0.88}Al_{0.12}O$ gate dielectric have been successfully fabricated by co-sputtering processes. Comparisons between device A and B as well as device B and C on electrical performance and threshold voltage shifts after gate bias and photo illumination tests have been demonstrated, which confirms the additive benefits of the Al incorporation into HfO_2 dielectric and Ti incorporation into IGZO channel in suppressing surface scattering and interface/bulk tap density. As compared with HfO_2/IGZO TFT, the proposed $Hf_{0.88}Al_{0.12}O$/Ti(2.0 %)-IGZO TFT shows a superior stability with ~78% and ~82% reduction in threshold voltage shift after 1000s PGBS/NGBS stress, respectively. It is expected that Al and Ti incorporation in IGZO-based TFT reported in this work could be potential for application in advanced displays.

Acknowledgements

This work was supported by the Ministry of Science and Technology (MOST), Taiwan, under contract MOST 104-2221-E-006130-MY3.

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