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Characterization of Asymmetry in Ni-Seed-Induced Laterally Crystallized (SILC) TFTs by New Gate-Floating-Drain-Current (GFDC) Method

Chris Chun-Chih Chung[1,(a)], Li-Chun Liu[1] and Tien-Sheng Chao[1,(b)]
[1] National Chiao Tung University.
1001 Ta Shueh Rd., Hsinchu City 30010, Taiwan (ROC)
[(a)]Phone: +886-972101817, E-mail: ccchung.311@gmail.com
[(b)]Phone: +886-3-5131367, E-mail: tschao@mail.nctu.edu.tw

Abstract

For the first time, asymmetry of Ni-Seed-Induced Laterally Crystallized (SILC) TFTs is identified and characterized by the new gate floating drain current (GFDC) method. For long channel device (L_g = 1.8 µm), the non-fully crystallized channel will result in electrical asymmetry in DIBL and I_{on} under source-drain reverse measurement. Grain boundary model is proposed to explain the phenomena. Finally, the asymmetry feature can be resolved by adopting shorter channel length (L_g = 0.35 µm) which renders better process and electrical performance stability with fully SILC TFTs.

1. Introduction

Low-Temperature-Poly-Silicon (LTPS) are vastly studied due to its higher mobility compared to amorphous silicon (a-Si) in active-matrix organic light-emitting diode (AMOLED) driving circuit applications [1]. Recently, it also raised great attention due to its better heterogeneous integration ability in 3D-ICs and IoT area [2].

Among various crystallization methods, Ni-Seed-Induced Lateral Crystallization (SILC) show great potential in crystallizing a-Si in low temperature (~500 °C), high throughput by furnace batch process, high mobility with pre-patterned active area that during crystallization the grain grows along channel direction [Fig. 1 (a)], and low leakage current due to low Ni contamination compared to conventional Ni-Metal-Induced Lateral Crystallization (MILC).

A self-aligned crystallization method will simplify the process but result in a wide grain boundary in the middle of channel which degrades the mobility; on the other hand, unidirectional method shows better performance [3], but the asymmetry electrical performance result from non-fully crystallized channel [Fig. 1 (b)] is a major problem for circuit level request. In this work, a device level measurement method is proposed that could identify the non-fully crystallized device.

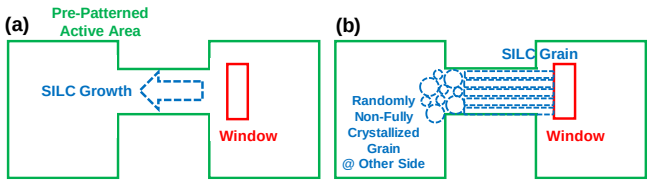

Fig. 1 (a) Pre-patterned active area and SILC growth direction are shown. The Window is where the Ni source is. (b) Non-fully crystallized grain at the other side is demonstrated.

2. Device Fabrication

Main fabrication processes are listed in Fig. 2 (a). After formation of 500 nm wet oxide and 100 nm SiN_x etching stop layer, a 50 nm a-Si was deposited as channel. Control samples are crystallized by solid phase crystallization (SPC) at this stage. Oxide hardmask and dummy Si is deposited and dummy region is patterned as shown in Fig. 2 (b). PE-TEOS oxide was conformally deposited and etched back to form spacer hardmask. Then the dummy Si was selectively removed [Fig. 2 (c)]. Source/Drain photoresist (PR) was defined and channel patterning was conducted in Fig. 2 (d). Active area was defined. On one of the S/D pad, a Window is defined by PR, then Ni was evaporated onto the wafer and patterned within the Window by lift-off process. And samples underwent the SPM (Piranha) clean with 90s leaving Ni-Seed in the Window [Fig. 2 (e)]. Then we use this Ni-Seed to laterally crystallize the channel at 500°C_N_2_12hr for 2 times just to rule out possible SPC under 500°C [Fig. 2 (f)]. After implantation and activation, IL/High-k/Metal Gate stack were deposited. The device was finished with gate patterning and gate spacer formation. Fig. 2 (g) is the top view of the device structure with red and green arrows showing the cross-section position with Fig. 2 (b-f)

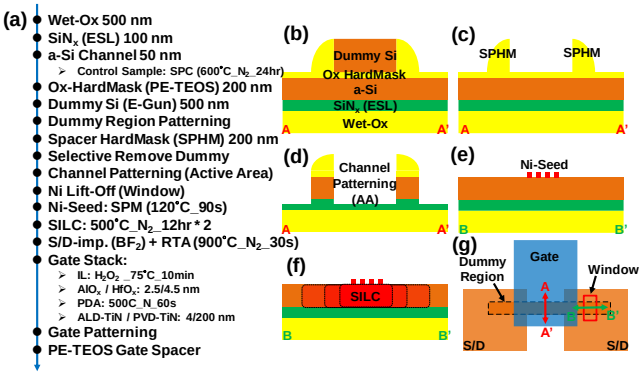

Fig. 2 (a) Main fabrication process. (b)Wet-Ox/ESL/a-Si (Channel)/Ox-HM/Dummy-Si deposition, dummy region patterning, SPHM formation. (c)Dummy region selectively removed. (d)Channel patterning with S/D-PR. Active area was defined. (e)Ni lift-off and clean by SPM leaving Ni-Seed at the Window. (f)SILC process. (g)Top view of the device structure. Cross-section A-A' and B-B' are shown in (b-f).

3. Result and Discussion

Asymmetry of Long Channel Devices (L = 1.80 µm)

For long channel devices with gate length of 1.8 µm, electrical characteristics asymmetry can be seen in DIBL and I_{on} as shown in Fig. 3 (a, b) with W-GND (Window Ground) and

W-BIAS (Window Bias) measurement condition, while control samples, crystallized by SPC, show no differences. For SILC, the longer the channel, the more it is susceptible to non-fully crystallization due to longer time needed for the NiSi front passing through the entire channel, also, the smaller the channel dimension, the longer time is needed to crystallize the channel according to Ma and Wong [4]. With the presence of non-fully crystallized grain at the edge of S/D, biasing at the Window side or the other will affect the electrical performance.

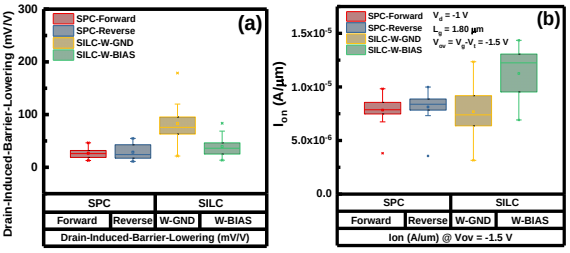

Fig. 3 (a) DIBL and (b) I_{on} comparison between SPC samples and SILC with W-GND and W-BIAS condition. For SILC, I_{on} is higher with W-BIAS due to less grain boundary at the Window side (Drain) where high lateral electric field drifts carriers.

Gate Floating Drain Current (GFDC) Measurement

In order to investigate the asymmetry phenomenon, gate floating drain current is measured with gate pin of the measurement system disconnected to the gate electrode of the device. As describe in Fig. 4, when large bias (V_d = -1 V) is applied to the non-fully crystallized side [W-GND] where there are more grain boundaries (GBs), potential barrier will be reduced with the bias which result in larger DIBL [Fig. 3(a)] and higher GFDC [Fig. 5] since hole carrier are prone to pass through the reduced barrier. On the other hand, under W-BIAS condition, DIBL is smaller due to better crystallinity and less GBs at the Window side and GFDC is lower due to the presence of blocking barriers at the other side [Fig. 5]. Fig. 5 (a) compares the GFDC of different device length under V_d = -1 V. We can see that as channel length is decreases, GFDC difference between W-GND and W-BIAS is reduced. It can be inferred that with shorter channel length, the whole channel is more likely to be fully crystallized. In Fig. 5 (b), under V_d = -0.1 V, due to the rather low voltage, barrier will not be greatly reduced rendering the same GFDC.

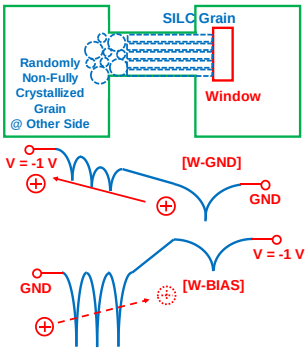

Fig. 4 Energy band-diagram of W-GND and W-BIAS condition. For W-GND, GBs at the non-fully crystallized side is reduced by bias while W-BIAS show no barrier lowering.

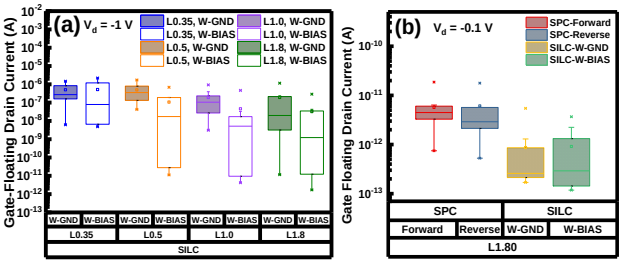

Fig. 5 (a) Gate floating drain current under V_d = -1 V. GFDC of W-BIAS is lower than W-GND, and the difference is reduced as the channel length decreases suggesting that the channel is fully crystallized. (b) GFDC under V_d = -0.1 V, showing no difference in long channel device.

Shorter Channel Device (L = 0.35 μm)

From Fig. 5 (a) we can see that the GFDC difference between W-GND and W-BIAS is reduced as the channel length is scaled down to 0.35 μm. It implies that for shorter channel device, SILC will go through the entire channel which will increase the stability of the process and the final electrical characteristics. Fig. 6 (a, b) show the DIBL and I_{on} with gate length of 0.35 μm. It is clear that no asymmetry is observed for W-GND and W-BIAS.

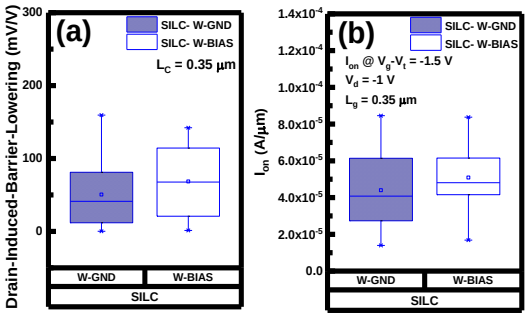

Fig. 6 (a) DIBL and (b) I_{on} of SILC device with channel length 0.35 μm. No difference is observed between W-GND and W-BIAS due to the fully crystallized channel.

4. Conclusions

The asymmetry of SILC TFTs is identified and characterized by new gate floating drain current method for the first time. As described by the band-diagram, the asymmetry of device performance and GFDC is due to the non-fully crystallized grain boundary at the other side of channel. For shorter channel the problem can be resolved. It also has the advantage of process and electrical performance stability.

Acknowledgements

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