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Hole Mobility Enhancement Observed in (110)-Oriented Strained Si

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Abstract

A significant enhancement of the effective hole mobility in a (110)-oriented strained Si pMOSFET was demonstrated. It was revealed that the anisotropic aspects of strain and defect formation are relevant to the hole mobility enhancement.

1. Introduction

In order to pursue further improvement of performance of semiconductor devices, development of novel materials is desired. The carrier mobility is a key material property which determines device performances and power consumption. Therefore, a number of studies have been carried out on high-mobility semiconductor materials such as Ge. As a matter of fact, the effective hole mobility exceeding 500 cm^2/Vs was reported in Ge-based MOSFET device [1] [2]. On the other hand, controls of defect formation and strain are also important techniques which increase the possibility of further improvement of the semiconductor device performances. Although numerous studies have been carried out on these topics, strained heterostructure systems on non-(100) substrates still need investigations. According to a computational study, a significant enhancement of the hole mobility is expected on (110)-oriented strained Si [3]. We have shown that defect morphology and strain in this material system are significantly anisotropic [4]. We also showed that quality of the material significantly depends on crystal growth conditions [5]. These aspects are unique to the (110)-oriented system and consequences of them on the carrier mobility needs to be investigated. In this study, we report on a significant enhancement of hole mobility in a (110)-oriented strained Si film. The effective mobility as high as 480 cm^2/Vs was achieved. The significances of strain and anisotropic formation of defects are discussed.

2. Results and Discussion

Strained Si/SiGe heterostructures were grown on a Si(110) substrate using the solid-source MBE method. The composition grading technique was employed to form the SiGe layer. The substrate temperature during the growth was 600 °C. After the growth, rapid thermal annealing at 800 °C for 1 min was performed under Ar atmosphere. Under these conditions, microtwins parallel to the $[\bar{1}10]$ direction predominantly generate [6]. These microtwins are equivalent to the stacks of partial dislocations with the Burgers vector a/6[112]. Therefore, the strain in the SiGe layer relaxes mainly in the [001] direction, which is confirmed by x-ray diffraction measurements. Accordingly, the top Si layer is fully strained in the [001] direction and unstrained in the $[\bar{1}10]$ direction. Fig. 1 shows AFM image. Reflecting the anisotropy in the defect formation, surface morphology is also directional. Striations extending in the $[\bar{1}10]$ direction are relevant to the microtwins below the surface [6]. A p-MOSFET having the channel direction in the $[\bar{1}10]$ direction was fabricated on the grown film using conventional photolithography technique. The effective hole mobility was evaluated by utilizing IV and split-CV measurements. Fig. 2 shows results of IV measurements. It is seen that the drain current of the strained Si MOSFET is significantly high compared to that of the Si(110) p-MOSFET control sample. The results of the CV measurements are plotted in Fig. 3. Also plotted in Fig. 3 are drain conductance vs gate voltage curves which were derived from the IV measurements. It is seen that the onset gate voltages of the CV curves coincide with those of the drain conductance curves. This means that the measured capacitance can be simply attributed to the inversion charge. Also, the capacitance values at on/off conditions are correspondent with the areas of the channel and the gate-SD overlap regions. Both IV and CV data indicate that the carrier distribution in the device region is well-modulated by the gate voltage. Fig. 4 shows the derived effective hole mobilities as functions of hole density. It is seen that the hole mobility is significantly enhanced in the (110)-oriented strained Si sample. The maximum hole mobility is 480 cm^2/Vs which is almost comparable with those of Ge-based devices. There are two conceivable mechanisms of the hole mobility enhancement. First, the hole effective mass is low in the (110) oriented tensile-strained layer [3]. Secondly, the microtwins and surface striation are significantly directional so that the carrier scattering rate is expected to be low in the $[\bar{1}10]$ direction. In addition, the valence band edge of the (110)-oriented strained Si lies above that of the SiGe buffer layer when the strain is anisotropic [6]. Due to this condition, holes are effectively attracted to the high-mobility layer in the inversion condition, and undesired leakage current through the SiGe layer can be suppressed.

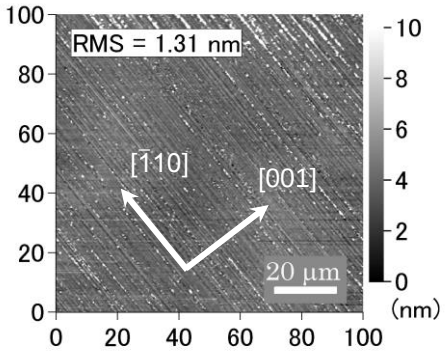

Fig. 1 AFM image.

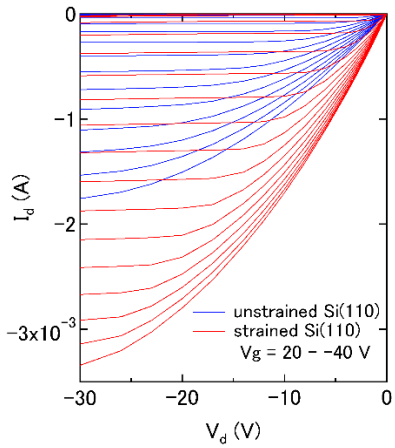

Fig. 2 Results of IV measurements.

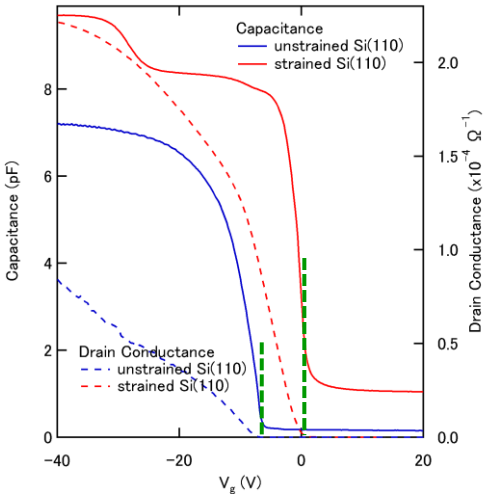

Fig. 3 Dependences of gate capacitance and drain conductance on the gate voltage.

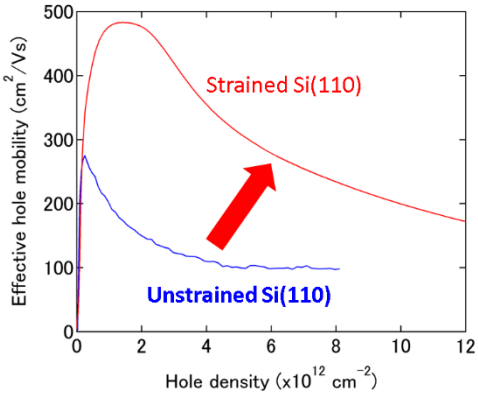

Fig. 4 Results of IV measurements.

3. Conclusions

A significant enhancement of the effective hole mobility was demonstrated on a (110)-oriented Si pMOSFET. The results of this study indicate the feasibility of higher-performance semiconductor circuits on cost-effective Si platforms.

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