

## Low-Temperature Bi-Induced Layer Exchange Crystallization for Formation of n-Type Ge on Insulator

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### Abstract

**Low-temperature ( $\leq 500^\circ\text{C}$ ) formation of n-type crystalline Ge (free electron concentration:  $>1 \times 10^{19} \text{ cm}^{-3}$ ) on insulator is desired to merge optical devices onto large-scale integrated circuits. To achieve this, layer-exchange crystallization using a-Ge/Bi stacked structures is investigated. Annealing ( $\geq 270^\circ\text{C}$ , 20 h) of a-Ge/Bi stacked structures triggers layer exchange growth of Ge. The electrical properties of grown films significantly depend on the annealing temperature. By selecting an annealing temperature of  $300^\circ\text{C}$ , n-type Ge (free electron concentration:  $\sim 7 \times 10^{19} \text{ cm}^{-3}$ ) is realized.**

### 1. Introduction

A low temperature ( $\leq 500^\circ\text{C}$ ) growth technique of n-type Ge (free electron concentration:  $>1 \times 10^{19} \text{ cm}^{-3}$ ) on insulator is necessary to realize the next-generation large-scale integrated circuits (LSIs), where optical functions are merged. This is because n-type Ge (free electron concentration:  $>1 \times 10^{19} \text{ cm}^{-3}$ ) shows high-efficiency optical functions owing to high electron population in the  $\Gamma$  band [1].

To achieve crystalline Ge films on insulator at low-temperatures, various techniques, e.g., solid-phase crystallization (SPC) and metal-induced layer-exchange crystallization (MIC), have been developed [2]. Among these techniques, MIC enables formation of orientation-controlled large grains ( $\geq 50 \text{ }\mu\text{m}$ ), by combining with a nucleation control technique [2]. However, most of the films grown by MIC techniques show p-type conduction, due to residual metals and vacancy-related defects in grown layers. We previously reported MIC using a group V element (Sb) and obtained n-type Ge [3]. However, the free electron concentration was low ( $\sim 2 \times 10^{17} \text{ cm}^{-3}$ ).

In the present study, we investigate MIC using another group V element (Bi) as a catalyst. Formation of n-type Ge with a high free electron ( $\sim 7 \times 10^{19} \text{ cm}^{-3}$ ) is realized by selecting the annealing temperature ( $\sim 300^\circ\text{C}$ ).

### 2. Experiments and Results

The sample structure is illustrated in Fig 1. In the experiment, fused-quartz (amorphous  $\text{SiO}_2$ ) chips were utilized as substrates. Stacked structures of a-Ge (thickness: 100 nm)/Bi (thickness: 100 nm) were formed on the substrates. The samples were annealed at  $250^\circ\text{C}$ – $350^\circ\text{C}$  for 20 h in  $\text{N}_2$  to induced crystallization. The grown layers were analyzed by micro-probe Raman

spectroscopy, Auger electron spectroscopy (AES), and Hall effects measurements.

The Raman spectra of samples before and after annealing at  $250^\circ\text{C}$ – $300^\circ\text{C}$  are shown in Fig. 2. Here, the measurements were performed from the back-side of the samples through transparent quartz substrates, as well as from the top-side of the samples. Before annealing, no Raman peak is detected. After annealing at  $250^\circ\text{C}$ , a small peak due to Ge-Ge bonding in crystalline Ge appears at  $\sim 300 \text{ cm}^{-1}$  from the back-side, which suggests initiation of layer-exchange growth. For annealing temperatures above  $270^\circ\text{C}$ , the Raman peaks due to Ge-Ge bonding observed from the back-side become very large. On the other hand, the Raman peaks are also observed from the top-side after annealing at temperatures above  $\sim 270^\circ\text{C}$ .

To reveal the phenomena, composition profiles for samples before and after annealing were analyzed using AES. The results are summarized in Fig. 3, where the x-axes are sputtering time. Before annealing, a stacked structure of Ge and Bi is formed, as shown in Fig. 3(a). Fig. 3(a) indicates that the region of Ge is wider than that of Bi. This is attributed to that the sputtering rate of Bi is significantly larger compared with Ge. The composition profiles after annealing at  $250^\circ\text{C}$  are almost the same as those before annealing. On the other hand, after annealing at  $270^\circ\text{C}$ , the Bi concentration is increased to  $\sim 30\%$  in the surface region (etching time  $< 100 \text{ s}$ ), while the Ge concentration is increased to  $\sim 100\%$  near the bottom interface (etching time:  $\sim 200 \text{ s}$ ). After annealing at  $300^\circ\text{C}$ , the concentration of Ge in the bottom region (etching time: 100–200 s) is increased to above  $\sim 80\%$ . These results indicate that the layer-exchange reaction is triggered by annealing at temperatures above  $270^\circ\text{C}$ . However, a large amount of Ge atoms ( $\sim 70\%$ ) remain in the surface region. These results agree with the Raman spectra obtained from the top-side after annealing at temperatures above  $270^\circ\text{C}$ , where peaks due to Ge-Ge bonding are observed. We speculate that Bi atoms, which moved to the surface regions, are partially evaporated during the annealing, and thus, the surface region becomes Ge-rich.

The electrical properties of the grown layers are investigated by Hall effect measurements. The results are summarized as a function of the annealing temperature in Fig. 4(a). The conductive types of the grown layers depend on the annealing temperature. For annealing temperatures between  $250$ – $270^\circ\text{C}$ , the grown layers show p-type, where the carrier concentrations are almost

constant ( $\sim 2 \times 10^{19} \text{ cm}^{-3}$ ), and the mobility decreases from  $\sim 140$  to  $\sim 30 \text{ cm}^2/\text{Vs}$  with increasing annealing temperature. At an annealing temperature of  $\sim 300^\circ\text{C}$ , the grown layers show n-type with the carrier concentration of  $\sim 7 \times 10^{19} \text{ cm}^{-3}$  and the mobility of  $\sim 5 \text{ cm}^2/\text{Vs}$ . For annealing temperatures of  $\sim 350^\circ\text{C}$ , the grown layers again show p-type, which is probably due to phase separation of Ge and Bi by eutectic reaction.

The free electron concentration obtained at  $300^\circ\text{C}$  in the present study is compared with thermal equilibrium solid-solubility of Bi in Ge in Fig. 4(b), where the broken line shows extrapolation of reported values of Bi solubility [4]. It is found that the free electron concentration obtained in the present study is significantly higher compared with the solubility of Bi at  $300^\circ\text{C}$ . Further study is needed to reveal the origin of the high free electron concentration ( $\sim 7 \times 10^{19} \text{ cm}^{-3}$ ).

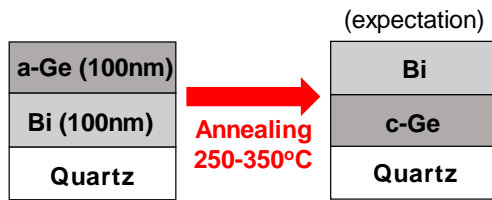


Fig. 1. Schematic sample structure.

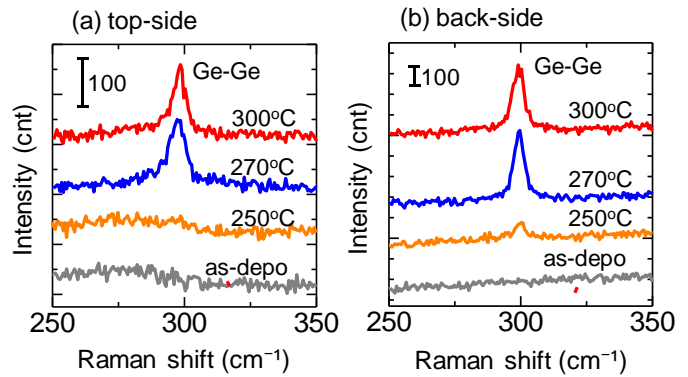


Fig. 2. Raman spectra obtained from top-side (a) and back-side (b) of samples before and after annealing.

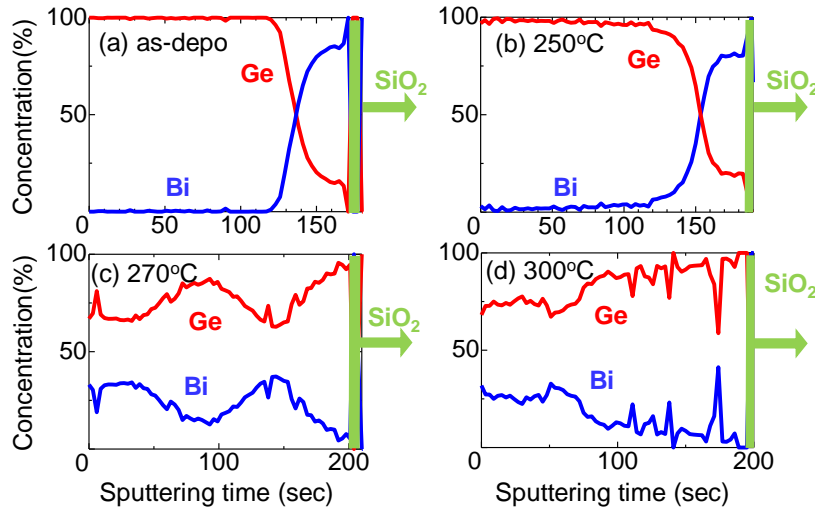


Fig. 3. In-depth profiles of Ge and Bi concentrations in samples before and after annealing.

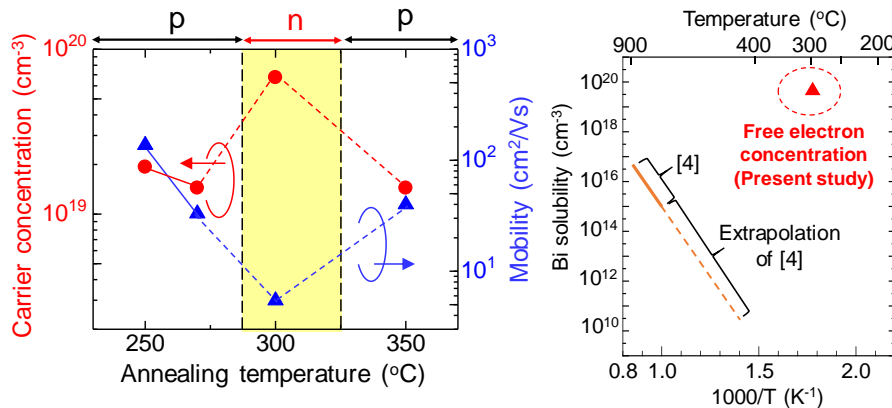


Fig. 4. (a) Annealing temperature dependence of carrier concentration and mobility in grown films and (b) comparison between free electron concentration and thermal equilibrium solid-solubility of Bi in Ge.

### 3. Conclusion

Low-temperature Bi-induced crystallization of Ge on insulator has been developed. Layer exchange reaction is initiated by annealing above  $\sim 270^\circ\text{C}$ . The electrical properties of the grown layers significantly depend on the annealing temperature. As a result, n-type Ge (free electron concentration:  $\sim 7 \times 10^{19} \text{ cm}^{-3}$ ) is obtained at  $\sim 300^\circ\text{C}$ . This technique will be useful for realization of advanced LSI combined with optical functions.

### References

- [1] X. Sun, et al., APL **95**, 011911 (2009).
- [2] M. Miyao et al., JJAP **56**, 05DA06 (2017).
- [3] H. Gao, et al., SSDM E-6-02 (2018).
- [4] F. Trumbore, et al., JECS **109**, 734 (1962).