Development of PCM and OTS combined Macro-models for HSPICE Compatible Simulation

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Abstract

PRAMs with PCM and OTS have been reported and applied for the crossbar array structure. The characteristics of PCM and OTS have significant effects on the PRAM operation. This paper introduces a novel PCM and OTS combine macro-model based on the physical mechanisms of them. The combined macro-model includes several intermediate states of PCM and turn on, off of OTS occurring during memory operation. This allows designers to understand the device behavior accurately and design more reliable PRAM after considering various device effects.

(Keywords: PRAM, PCM, OTS, Macro-model)

1.Introduction

Phase-change Random Access Memory (PRAM) is a one of the most promising candidates for next generation memory with non-volatility, high cycling endurance, low read/write latency and high scalability. As shown in Fig. 1, PRAM consists of Phase-Changing Materials (PCM) and Ovonic Threshold Switching (OTS) between bitlines (BLs) and wordlines (WLs). The resistance of PCM is determined by the crystallization state of PCM (i.e. crystalized state and amorphous state). PRAMs with crossbar array architecture have been investigated for achieving higher memory density. Here, OTS devices operate as selectors [1]. Since both PCM and OTS are resistive devices, variations in them affect PRAM operation substantially [2]. Therefore, it is essential to consider both PCM and OTS characteristics while designing PRAM programming and sensing circuits. There are several PCM models that has been reported [3-4], but OTS model is not considered, also the combine of both PCM and OTS is not considered. Therefore, it is highly necessary to develop macro-models of both devices that are compatible to the HSPICE simulator. In this work, we explain PCM and OTS characteristics, and present PCM and OTS macro-models and combined macro-models using Verilog-A.

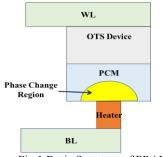
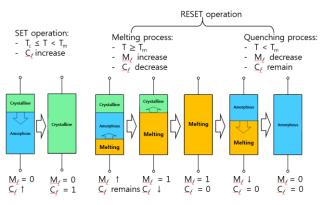


Fig.1 Basic Structure of PRAM



 $\label{eq:Fig.2} \begin{array}{l} \mbox{Fig.2 Operation of PCM Macro-model Crystalline fraction}(C_f), \\ \mbox{melting fraction}(M_f) \end{array}$

2.Proposed macro-model

The proposed PCM model controls the read and write operation, changing states, and resistance by input signals. Various parameters such as the PCM state and the PCM resistance with variations can be read out from the model for Hspice simulation. The developed PCM model also supports resistance variations and multi-level PCM states, which helps to verify the impacts of multiple cell states or the resistance variations during PRAM operation.

PCM marco-model

Fig. 2 shows the operation of the proposed PCM macromodel. When bias is applied, the temperature of PCM is calculated, and the crystalline fraction (C_f) and the melting fraction (M_f) change according to the calculated temperature. Finally, the PCM resistance is calculated using C_f and M_f . Fig. 3 shows a transient simulation result of the developed PCM macro-model using the set bias of 1.5 V and the reset bias of 3V. As illustrated, C_f and M_f change depending on the amplitude of the applied bias and the duration. This generates three different PCM states, fully set, partially set, and reset.

OTS marco-model

Fig.4 show the operation of proposed OTS macro-model. The proposed OTS model is designed to realize the on-off switching characteristics according to the OTS bias voltage (V_{b} _OTS) between PCM and OTS. It is controlled by various input signals, such as voltages between top and bottom electrodes, and variation control signals. The model outputs transfer the data such as the on/off state and the OTS resistance to the schematic for Hspice simulation.

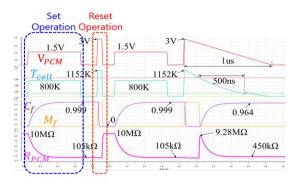


Fig.3 Reset and Set operation results of PCM model

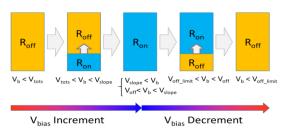
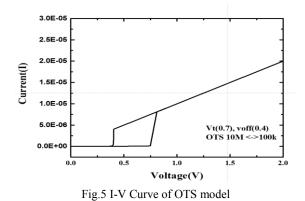


Fig.4 Realizing method of OTS turn-on slope

Fig.5 shows the I-V curve of proposed OTS model in linear. When V_{bias} exceeds V_t , the OTS macro-model demonstrates a short period of turn-on slope, followed by a complete on-state. When decreasing V_{bias} , the modeled OTS remains turned on until V_{bias} reaches V_{off} .



Combined PCM and OTS macro-model

Fig.6 show the operation of proposed combined PCM OTS macro-model. OTS and PCM is connected. when set and reset operation, V_{bias} is distributed to the resistance values of OTS and PCM, respectively. At this time, when the OTS voltage value exceeds V_t (0.7V), The OTS turns on and PCM set and reset operations occur. if OTS voltage value decease V_{off} (0.4V) Then OTS turn off, The PCM states are stored. read operation uses small V_{bias} and can be used to check the PCM states (set, reset) depending on whether the OTS is turned on (Low resistance state).

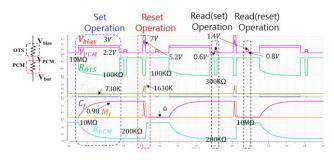


Fig.6 Reset and Set and read operation results of OTS and PCM combined model

3. Conclusion

In this paper, we proposed PCM and OTS Macro-model of various characteristic, such as PCM resistance, V_t , OTS ON/OFF characteristic, set, reset, read operation. The proposed OTS and PCM combined macro- model can provide advantages to circuit designers to design the read circuit and sense amplifiers for PRAM more accurate and overcome read errors various PRAM characteristics.

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