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Polycrystalline Silicon MOSFET-based Multi-Layer Capacitorless DRAM (1T-DRAM) for the Embedded System

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Abstract

In this paper, polycrystalline silicon (poly-Si) MOSFET-based multi-layer capacitorless DRAM (1T-DRAM) is proposed for embedded systems. Although the poly-Si-based devices have lower electron mobility than the single crystalline Si-based devices, the proposed device achieved high read current and high current margin (> 20 μA/μm) improved by multi-layer structure. In addition, even at the short gate length of 20 nm, high retention time (> 100 μsec) were obtained at T = 358 K. Furthermore, the excellent reliability for randomly generated grain boundaries was validated by the device simulations.

1. Introduction

Embedded dynamic random-access memory (eDRAM) is one of the most promising memory technologies for the successful system on chip (SoC) solutions [1]. However, the conventional 1T-1C DRAMs have the drawbacks of complex fabrication process and capacitor shrinking. Thus, there are considerable researches of eDRAM using capacitorless one transistor DRAM (1T-DRAM) due to its attractive advantages which is the simple fabrication and realization of three-dimensional (3-D) memories [2-3].

In this work, the polycrystalline silicon (poly-Si) MOSFET-based multi-layer (ML) 1T-DRAM has been studied. Recently, poly-Si has attracted attentions for the fabrication and implementation of 3-D ML stackable devices. Although poly-Si has disadvantage of low on-state current (I_{on}) due to the mobility and the grain boundary (GB) [4-5], the proposed device shows high read current and high current margin (CM) by 3-D structure with ML. In addition, in spite of the small dimension of the device, high retention time (RT) was achieved even at high temperature (T = 358 K). Furthermore, the proposed devices with ML structure demonstrated superior reliability in terms of memory operations for randomly distributed GBs.

2. Results and Discussion

Fig. 1 shows the schematics of the poly-Si MOSFET-based 1T-DRAM with stacked ML structure. The proposed device has the gate length (L_g) of 20 nm, the gate dielectric thickness (T_{ox}) of 3 nm, and the body thickness (T_{body}) of 12 nm. The gate metal thickness (T_{metal}) is 10 nm. The work functions of the gate for read operation and the control gate (CG)

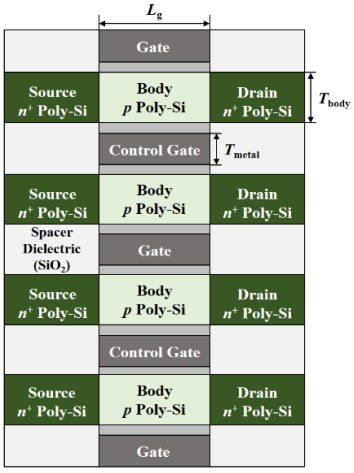
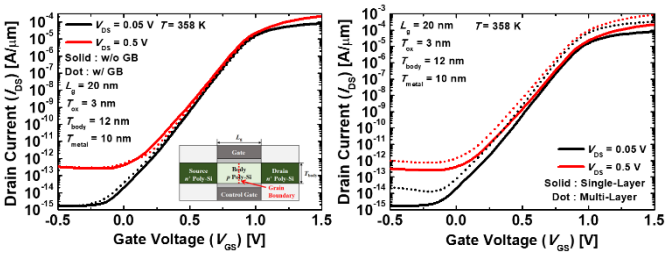


Fig. 1 Schematic view of the proposed poly-Si MOSFET-based 1T-DRAM with stacked multi-layer structure.



(a) (b)

Fig.2 Transfer characteristics of the (a) proposed SL 1T-DRAM and (b) both SL and ML 1T-DRAM at T = 358 K.

for write/erase operations are 4.8 eV and 5.3 eV, respectively. The doping concentrations of the source, body, and drain are n-type 10^{20} cm^{-3}, p-type 10^{18} cm^{-3}, and n-type 10^{20}cm^{-3}, respectively. For higher reliability, various models including Shockley-Read-Hall recombination, auger recombination, trap-assisted-tunneling, doping dependent mobility, bandgap narrowing, Fermi-Dirac statistics, quantum confinement effect, and non-local band-to-band tunneling were simultaneously used [6].

Fig. 2 (a) shows the transfer characteristics of the proposed single layer (SL) device at T = 358 K. As indicated in the figure, GB degrades the DC performances of the devices. However, regardless of GB, the device has low off-state current (I_{off}), and thus, low leakage current flows during a hold operation. And as shown in Fig. 2 (b), the proposed ML-based

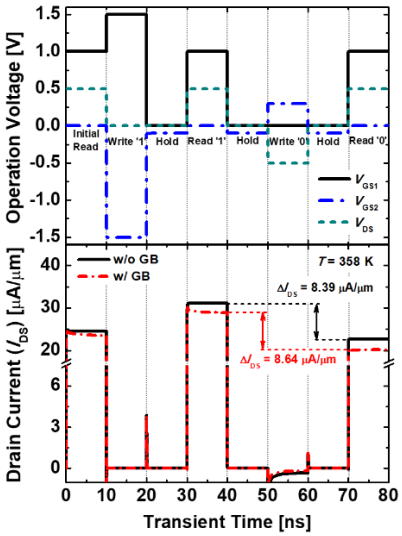
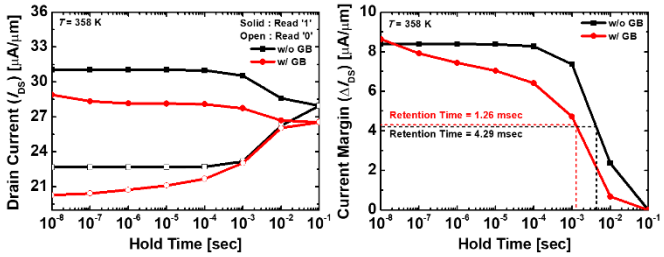
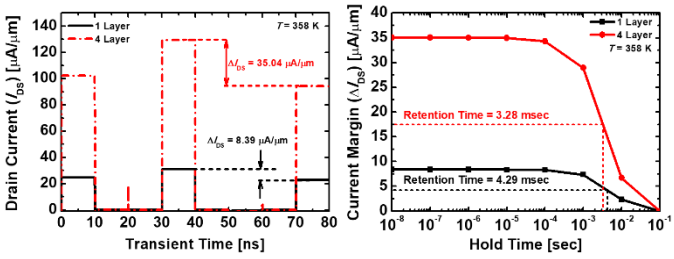


Fig.3 Operation bias scheme and memory operation of the proposed SL 1T-DRAM.



(a) (b)

Fig.4 (a) Read "1"/"0" currents and (b) current margin as a function of hold time.



(a) (b)

Fig.5 (a) Memory operation and (b) retention characteristics of the SL and ML 1T-DRAM.

device has superior I_{on} compared to I_{on} of SL structure.

Fig. 3 depicts the operation bias scheme and memory operation of the proposed 1T-DRAM with SL structure. The write operation is realized by the band-to-band tunneling. Erase operation is performed by applying V_{CG} = 0.3 V and V_{DS} = - 0.5 V. During hold operation, small negative voltage is applied at CG for holes storage near CG.

Fig. 4 (a) and (b) indicate read "1"/"0" currents and current margin as a function of hold time, respectively. Because of the low dimension of the proposed device, performances with only one GB were considered. Regardless of GB, the proposed devices have similar read current, CM, and RT which are excellent for the embedded systems.

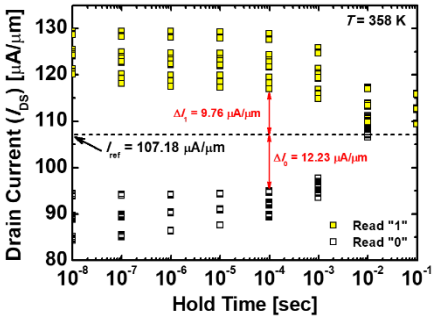


Fig. 6 Read "1"/"0" currents of the proposed devices with randomly distributed GBs.

Fig. 5 (a) shows the memory operation of the SL and ML 1T-DRAMs. It is confirmed that higher read currents and higher CM were obtained by ML structure. Fig. 5 (b) indicates retention characteristics of the SL and ML 1T-DRAMs. RT of both SL and ML 1T-DRAM exhibited excellent performances proper to the embedded systems.

Fig. 6 depicts read "1"/"0" currents of the ML 1T-DRAMs with random GB distributions. The reference current (I_{ref}) was set to intermediate value of minimum read "1" current and maximum read "0" current. The proposed devices have high RT (> 100 μsec) for all cases, demonstrating good reliability.

3. Conclusions

In this work, poly-Si MOSFET-based ML 1T-DRAM has been proposed and investigated. The proposed device achieved superior performances with high CM of 35.04 μA/μm, and high I_{on} of 94.9 μA/μm by ML structure, In addition, despite low dimension of L_g = 20 nm, high RT of 3.28 msec was obtained even at high temperature. Furthermore, the device has demonstrated excellent reliability for randomly generated GBs.

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