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Selectable Amplification of Sensor Using Coplanar Gate IGZO TFT with Variable Resistance Layer

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Abstract

In this study, we deveolped a sensor with a coplanar gate by using variable resistance layer in resistance coupling effect to decide sensitivity for various situation of sensing materials. The fabricated coplanar gate field-effect transistors (FETs) showed high resistance state (HRS), low resistance state (LRS) amplification of 1.76, 2.99 and linearity of more than 99%. Therefore, coplanar gate sensor that has selectable amplification in resistance coupling effect is expected to be a useful method for next generation IoT as well as various sensor model of new structure.

1. Introduction

Recent developments in Big Data, Artificial Intelligence, Deep Learning, and IoT in the 4th industrial Revolution have led to increasing interaction between humans and devices. Therefore, much research has been performed as interest in sensors has increased. However, the conventional FET has a low sensitivity at room temperature and disadvantage of a fixed sensirtivity. In order to onvercome this problem, we fabricated sensors has selectable amplification using changeable resistance layer. In this study, the variable resistance layer extracted the amplification factor of the sensing material potential of the thin film transistor for each state using the switching operation of the conventional resistance random access memory (ReRAM) [1].

2. General Instructions

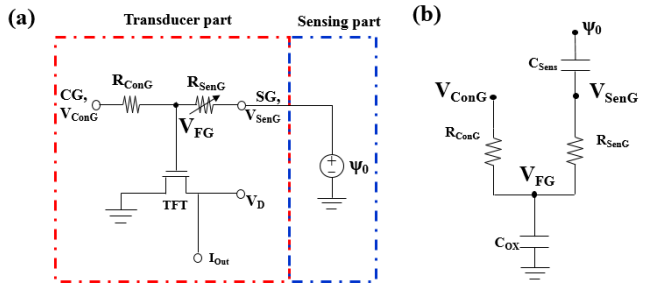

Fig.1 (a) the sensor circuit using the variable resistor in resistance coupling proposed in this study, and (b) is the circuit simplified from (a).

Where R_{ConG}, R_{SenG} is resistance of control gate (CG), sensing gate (SG). V_{FG}, V_D is front gate and drain voltage and I_{out} is drain current. Fig. 1 (a) is a sensor circuit using the variable resistor in resistance coupling proposed in this study, and (b) shows the circuit simplified from (a). First, V_{ConG} is the potential of control gate, which is the voltage change of the element to be detected. At this time, the parasitic resistors of the device are ignored. Fig. 1 (b), the V_{FG} can be expressed by the following equation (1).

$$V_{FG} = \frac{R_{ConG}}{R_{ConG}+R_{SenG}} V_{ConG} + \frac{R_{SenG}}{R_{ConG}+R_{SenG}} V_{SenG} \quad (1)$$

Equation (2) is summarized as follows for variation of sensing potential.

$$\Delta V_{FG} = \frac{R_{ConG}}{R_{ConG}+R_{SenG}} \Delta V_{ConG} + \frac{R_{SenG}}{R_{ConG}+R_{SenG}} \Delta V_{SenG} \quad (2)$$

The variation of the CG using equations (1) and (2) is summarized as follows equation (3).

$$V_{ConG}^{th} = \frac{R_{ConG}+R_{SenG}}{R_{ConG}} V_{FG}^{th} - \frac{R_{ConG}}{R_{SenG}} \Delta\psi_0 \quad (3)$$

Therefore, the V_{ConG}^{th} input to the CG increases the sensing stress R_{ConG}/R_{SenG} times, confirming that the very fine sensing stress, $\Delta\psi_0$, can be amplified and sensed through the resistance coupling effect

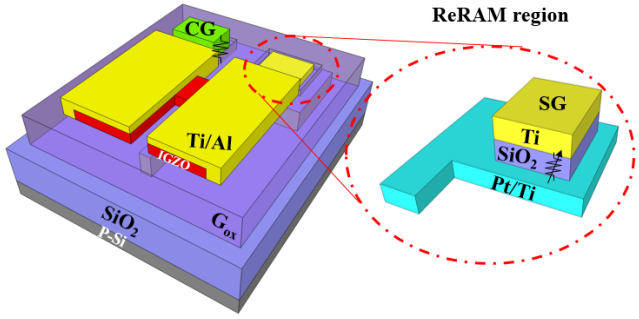

Fig. 2 Schematic illustrations of coplanar gate IGZO TFT with variable resistance layer.

Fig. 2 shows schematic of coplanar gate IGZO TFT with changeble resistance layer. First, Pt/ Ti (100/ 10 nm) are deposited on (100) p-type Si wafer by e-beam evaporation as the gate electrode. Then, a 100 nm thick of SiO_2 was deposited by RF magnetron sputtering to form the gate oxide. To form the ative channel layer, 50 nm thick of In-Ga-Zn-O (In_2O_3:Ga_2O_3:ZnO = 4:2:4.1 mol%, IGZO) was deposited and

defined by photolithography and Buffer oxide etchant (BOE) 30:1 solution. Then, Al/ Ti (100/ 2 nm) source/ drain (S/D) electrode were deposited by e-beam evaporation and photolithgraphy. The changaeble resistance coplanar gate layer were fomred by photolithography using image reverse method on the gate electrode. Then, SiO_2 gate oxide was etched by BOE 30:1 solution up to 50 nm for proper resistance change operation and Ti electrode deposited continuously. Finally, in order to remove defects in the channel, gate oxide, and interface, post deposition annealing was conducted by furnace at 400 °C for 30 m in N_2 ambient. All measurements were performed in a dark box to avoid light and electrical noise and were measured using an Aglient 4156B Precision Semiconducotr Parameter Analyzer instrument.

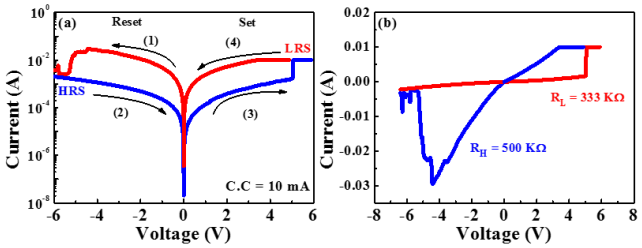

Fig. 3 Typical bipolar resistive switching behaviors in SG as (a) log scale and (b) linear scale for indicate the resistance in high and low resistance state.

Fig. 3 shows the bipolar resistive switching (BRS) characteristics in (a) log scale and (b) linear scale of SiO_2 50 nm ReRAM region. The BRS characteristics were measured by applying positive or negatives to the sensing gate and by grounding the transistor gate. When the compliance current (CC) is 10 mA. Fig. 3 (a) shows the BRS characteristics of Ti / SiO_2 / Pt ReRAM. The operation was operated in the order of the arrows. Fig. 3 (b) shows the resistance of each state and R_H of HRS has an average resistance of 500 KΩ, And the R_L of LRS showed an average resistance of 333 KΩ. We also confirmed the amplification of the variable resistor layer by applying the bias potential to the SG in each state.

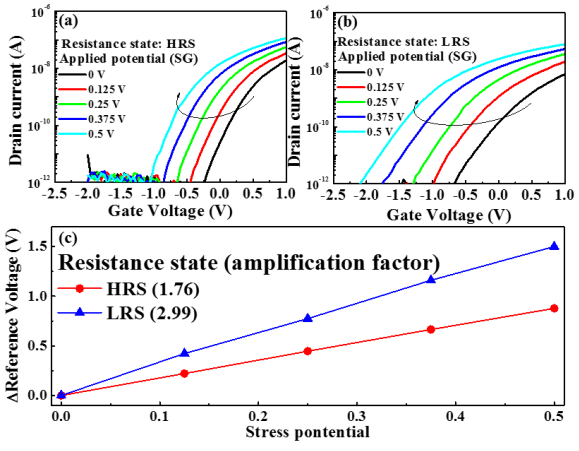

Fig. 4 I_D-V_G curves in (a) HRS, (b) LRS of sensing gate of coplanar IGZO TFTs and (c) change in reference voltage (V_R) according to applied potential in sensing gate for 0 to 0.5 V.

Fig. 4 shows the I_D-V_G curves in (a) HRS, (b) LRS of sensing gate of coplanar IGZO TFTs. As the applied potential to the SG increases from 0 to 0.5 V, the I_D-V_G curves shifted to negative direction. Fig. 4(c) shows shift of reference voltage with varying applied potential in SG. In the resistance of SG is low state (reset), the amplification factor is 1.76 and in the resistance of SG is high state (set), the amplification factor is amplified to 2.99. The resistance of SG in LRS is 333 KΩ and in HRS is 500 KΩ. This indicates that the amplification factor increased according to the resistance of SG decreased as shown in equation (3). Therefore, we can control the amplification factor through the resistance change operation of SG.

3. Conclusions

We proposed a resistance coupling effect and fabricated a coplaner gate using resistance coupling effect to measure the amplification according to various resistance ratios. Based on the simulation results, V_{in} could amplify the sensing stress of R_1/R_2 times and showed higher amplification. Therefore, it is expected that the coplanar gate ISFET using the resistance coupling effect of selective amplification proposed in this paper can be applied to various transistor based devices beyond the existing DG, and thus it will be used variously in IoT based sensors.

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[1] Oh, H. R., Cho, B. H., Cho, W. Y., Kang, S., Choi, B. G., Kim, H. J., … & Jeong, G. T., IEEE Journal of Solid-State Circuits 41(1) 122-126 (2005)