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Turn-Off Loss Improvement by IGBT Scaling

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Abstract

Effects of IGBT scaling on turn-off characteristics were studied by TCAD simulations. It was found that the scaling can reduce turn-off loss without degrading on-state loss (Vce_{sat}), owing to stronger IE effect (*i.e.* higher top side carrier concentration) and improved resistance to dynamic avalanche.

1. Introduction

Power semiconductor devices are key components of the modern industry. Among them, Insulated Gate Bipolar Transistors (IGBTs) [1,2] are widely used for high power applications. Recently, an IGBT scaling concept [3] has been proposed. It is reported that, by scaling down the dimensions of the trench-gated emitter both vertically and horizontally, on-state voltage (Vce_{sat}) can be reduced [3,5], owing to the injection enhancement (IE) effect [4]. In addition, it was experimentally demonstrated that the IGBT scaling also decreases turn-off loss [6,7], though the reason for this was not fully understood. Therefore, in this work, TCAD simulations were performed to clarify the effects of IGBT scaling on turn-off loss.

2. Analysis Method

Reference (k=1) and scaled (k=3) 3.3 kV class IGBTs (Fig.1) were simulated. The topside MOS structure dimensions were scaled by 1/3, though the trench width was kept constant to align with experiments [7]. The gate oxide thicknesses for k=1 and k=3 were 100 nm and 33 nm, respectively. Carrier lifetime was assumed to be independent from k. At the backside, a field stop structure was adopted, and the P-collector boron concentration was varied. Turn-off characteristics were analyzed in an inductive load circuit with 1700 V operation voltage (Vcc) and 80 A current (Io). Parasitic components were ignored. Gate voltage source swings of k=1 and k=3 IGBTs were ±15 V and ±5 V, respectively.

3. Analysis Results

Fig.2 shows typical on-state I-V characteristics as well as Vce_{sat} dependence on P-collector doping. Vce_{sat}, which determines the on-state power loss, is improved by the scaling thanks to the enhanced IE effect.

Fig.3 (a) shows typical turn-off waveforms for different collector voltage rising rates (dV/dt), which can be increased by reducing the gate series resistance. Turn-off loss $Eoff$ is given as the sum of Evr and Ecf (Fig.3 (b)). Higher dV/dt is beneficial for reducing Evr. However, Fig.3 shows that, while normal operation is realized when dV/dt=1 kV/μs, too large dV/dt=2 kV/μs causes an early Vge drop and inflection of the Vce vs time waveform. These are the indication of dynamic avalanche (DA); Due to the limited carrier velocity, too fast voltage swing results in insufficient depletion layer expansion and impact ionization. Fig.4 shows that holes are generated near the trench bottom when the avalanche starts. DA must be avoided for reliable operations, and will set a limit on the turn-off speed.

Evr and Ecf were calculated by systematically varying dV/dt and P-collector doping for both k=1 and 3 (Figs.5 and 6). Fig.5 shows that Evr does not depend on k, and is simply inversely proportional to dV/dt, as long as DA is not present. However, there is a major difference that the onset dV/dt of DA for k=3 is much larger than that for k=1. It is speculated that the reduced mesa width relieved the field confinement near the trench bottom. Fig.6 shows that Ecf, that is governed by the amount of stored carrier near the P-collector, increases approximately in proportion to P-collector doping and dV/dt. It is considered that large dV/dt will hinder transport of back side carrier to the front side, resulting in increased stored carrier concentration.

Fig.7 shows $Eoff$=Evr+Ecf vs Vce_{sat} relationships converted from the data in Figs.2, 5 and 6. When dV/dt=1 kV/μs, though Evr~100mJ dominates, k=3 devices show lower $Eoff$ due to reduced Ecf. This is because, a k=3 device can achieve equal Vce_{sat} as k=1 by lower P-collector doping due to the enhanced IE effect, which results in lower amount of back side stored carrier (Fig.8). The difference between k=1 and 3 becomes more pronounced when dV/dt=2 kV/μs, since Ecf is reduced. In addition, a k=3 device can achieve much lower Vce_{sat} than k=3 without suffering from DA.

4. Conclusions

Effects of IGBT scaling on turn-off loss were systematically studied using TCAD simulations. It was shown that the scaling is beneficial, not only for improving on-state loss, but also for reducing turn-off loss, owing to stronger IE effect and larger tolerance to dynamic avalanche.

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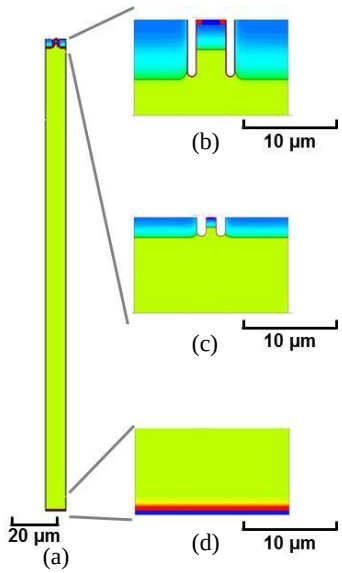

Fig.1 Simulated IGBT structure: (a) whole view, (b) k=1 top side, (c) k=3 top side, (d) bottom side.

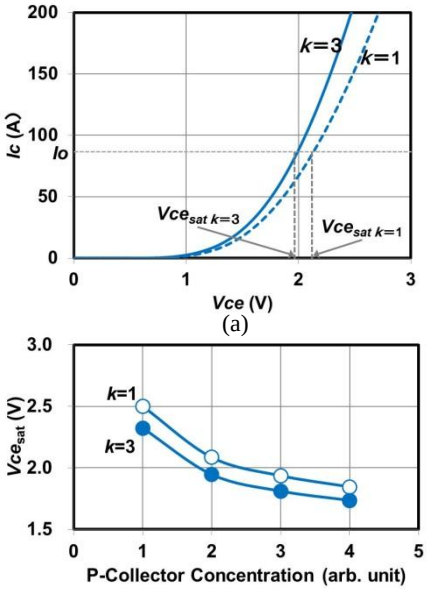

Fig.2 On-state characteristics: (a) typical *I-V*, and (b) Vce_{sat} vs. P-collector concentration.

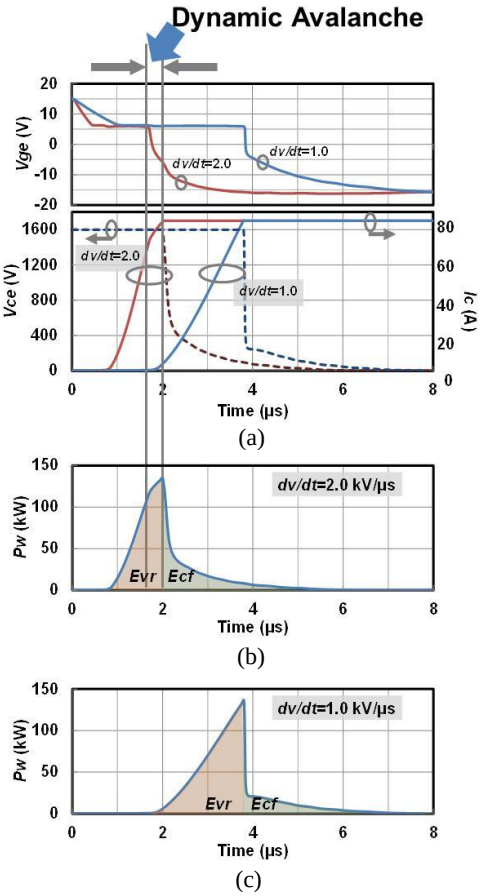

Fig3 Typical turn-off waveforms of k=1 IGBT: (a) *Vge*, *Vce* and *Ic*, vs. time, and power dissipation vs. time for (b) *dV/dt*=2.0 kV/μs, and (c) *dV/dt*=1.0 kV/μs.

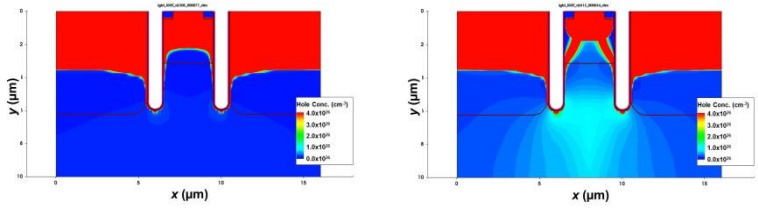

Fig.4 Hole distributions near emitter of k=1 IGBT at the moment of abrupt gate voltage drop, for (a) *dV/dt*=1 kV/μs, and (b) *dV/dt*=2 kV/μs.

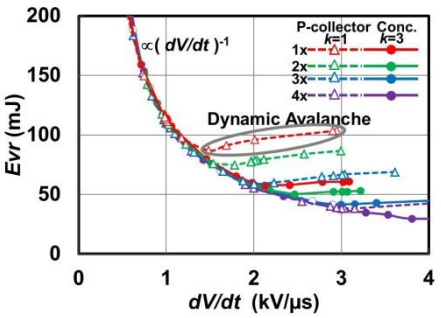

Fig.5 Dependence of *Evr* on *dV/dt*.

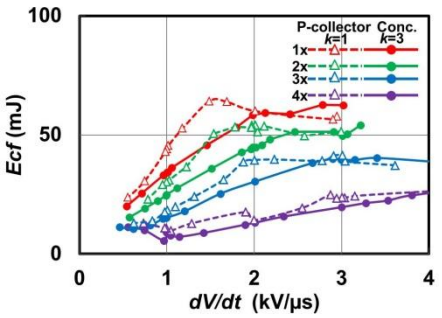

Fig.6 Dependence of *Ecf* on *dV/dt*.

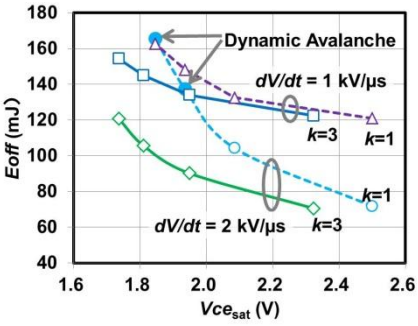

Fig.7 Trade off between *Eoff* and Vce_{sat}.

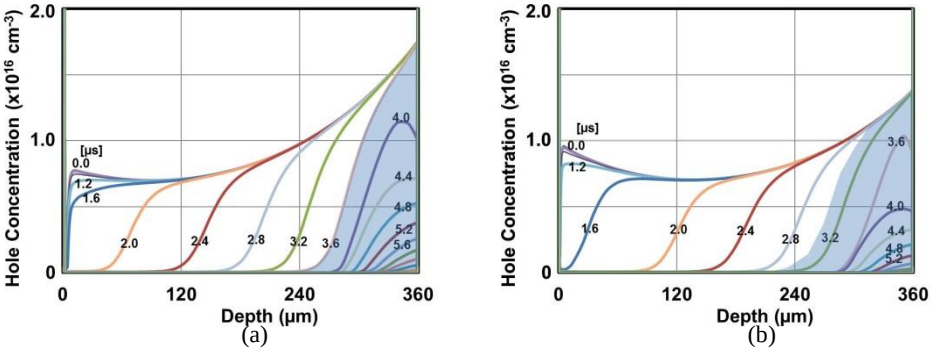

Fig.8 Hole distributions during turn-off process for (a) k=1 and (b) k=3. *dV/dt*=1 kV/μs, Vce_{sat}=1.95V, normal operation cases without DA for both devices. Hatched areas show stored carrier distributions at gate voltage drop.