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Demonstration of m-plane GaN metal-oxide-semiconductor field-effect transistors

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Abstract

We report on the first demonstration of lateral metal-oxide-semiconductor field-effect transistors (MOSFETs) with a m-plane GaN (1-100) channel. The Si-doped GaN layers exhibit an ohmic behavior, showing the specific contact resistivity of 2×10^{-5} Ωcm^2 and sheet resistance of 609 Ω/□. At the SiO_2/m-plane GaN interface, the interface state density shows 1.3×10^{11} cm^{-2}/eV. The Mg-doped GaN back-barrier layer suppresses the buffer-leakage current, providing good drain current saturation and stable pinch-off operation. The m-plane GaN MOSFETs show the transistor on/off ratio of ~10^5.

1. Introduction

GaN is an attractive material for high-power applications due to its high critical electric field and a large band-gap energy of 3.4 eV. Generally, c-plane GaN is used for devices due to the high crystalline quality and commercially available large-size bulks. Recently, GaN vertical-trench MOSFETs with the blocking voltage over 1 kV are reported.[1,2)] The trench MOSFETs are switched on/off using the m-plane MOS sidewall. However, the interface status between dielectric and m-plane GaN has been unveiled. In this study, we report on the evaluation of the SiO_2/m-plane GaN interface status and the demonstration of m-plane GaN-channel MOSFETs.

2. Experimental procedures

We used m-plane GaN (1-100) free-standing substrates. Using MOVPE, 30-nm-thick Si-doped GaN / 500-nm-thick unintentional-doped (UID) GaN / 1-μm-thick Mg-doped GaN / 1.5-μm-thick UID GaN layers were grown on the substrates at 1050°C. Impurity concentrations were determined by secondary-ion mass spectroscopy (SIMS). Detection limits for silicon, carbon, hydrogen were 5×10^{14}, 3×10^{15}, and 3×10^{16} cm^{-3}, respectively. The UID GaN layer has silicon, carbon, and hydrogen concentration under the detection limits and oxygen concentration of 3×10^{16} cm^{-3}. The silicon concentration in the Si-doped GaN layer and magnesium concentration in the Mg-doped GaN layer were 3×10^{18} and 5×10^{18} cm^{-3}, respectively. The net donor concentrations in the Si-doped and UID GaN layers was 2×10^{18} and 8×10^{17} cm^{-3}, respectively, which were determined by capacitance-voltage (*C-V*) measurements.

The fabricated m-plane GaN MOSFETs are schematically shown in Fig. 1. A 700-nm-deep mesa isolation was obtained by Cl_2-based reactive-ion etching (RIE) using a 50-nm-thick nickel metal mask. A Ti (20 nm)/Al (100 nm)/Ni (10 nm)/Au (50 nm) metal stacks were deposited using an electron-beam evaporation for source/drain contacts, followed by annealing at 800°C for 30 s in a nitrogen ambient to form metal alloy. The Si-doped GaN layer was etched by Cl_2-RIE, followed by the deposition of 20-nm-thick SiO_2 (TEOS) and Ni (30 nm)/Au (50 nm) metal stacks for gate. Finally, the dielectric on source/drain contacts was etched by CF_4-RIE. *C-V* and current-voltage (*I-V*) measurements were performed at room temperature using an Agilent B1500A analyzer.

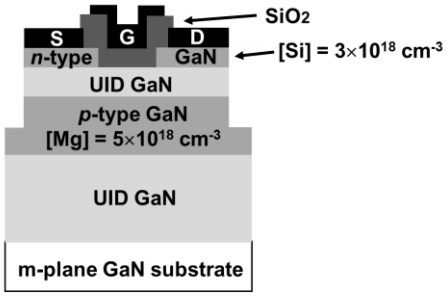

Fig. 1: Schematic cross section of *n*-channel m-plane GaN MOSFET.

3. Results and discussion

Electrical property of n-type GaN layer

Two Ti/Al/Ni/Au contacts separated by various source-drain spacing (L_{sd}) were used for a transmission line measurement (TLM). The Si-doped GaN layers were conductive at room temperature and were electrically isolated by the bottom Mg-doped GaN layers. Using TLM, the specific contact resistance R_c and sheet resistance R_{sh} of the Si-doped GaN layer parallel to the [0001] direction is estimated to be 2×10^{-5} Ωcm^2 and 609 Ω/□, respectively.

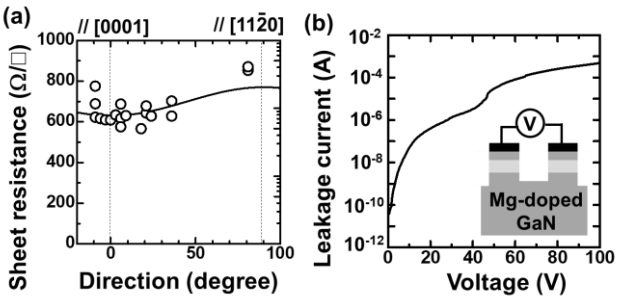

Fig. 2: (a) Dependence of sheet resistance on crystal orientation of Si-doped GaN layers with a donor concentration of 2×10^{18} cm^{-3}. (b) Two-terminal buffer-leakage current of Mg-doped GaN layers.

The dependence of R_{sh} on the crystal orientation of the Si-doped GaN layer are shown in Fig. 2 (a). R_{sh} parallel to the [0001] direction was slightly lower than that parallel to the [11-20] direction. The anisotropy of R_{sh} is derived from the anisotropies of the film mosaic and effective electron mass.[3] The fitted curve using m_c/m_a=1.1 is in good agreement with the experimental data, indicating that the effective electron mass dominantly affects the different R_{sh}.

We investigated the *I-V* characteristic through the Mg-doped GaN layer, as shown in Fig. 2 (b). The leakage current dramatically increases at the reverse bias of -10 V. The reduction of the unintentional oxygen incorporation and increase of the acceptor concentrations in the Mg-doped GaN layer would reduce the leakage current.

Interface state density of SiO_2/m-plane GaN interface

The high-frequency *C-V* curves of SiO_2/GaN MOS capacitors patterned by a circle shape with a diameter of 50 μm are shown in Fig. 3 (a). The voltage was swept from the depletion region to the accumulation region, clearly showing a deep depletion behavior due to the low minority-carrier generation rate of GaN. The effective thickness of the insulater layer was estimated to be 17 nm from the capacitance in the accumulation region, being close to the SiO_2 thickness. The flat band voltage is 0.8 V for 100 kHz. The *C-V* curve from the accumulation region to the depletion region is shifted toward the positive direction with increasing frequency. This results from the increase of electron trapped in shallow interface states at the higher frequency.

The dispersion in the *C-V* curves was observed, indicating that interface states induced by the RIE damage and surface impurities respond to the high frequency. The total hysteresis window at the flat band is 1.3 V, estimating to be the effective interface-state density of 1.3×10^{11} cm^{-2}/eV. This value is comparable to that for the SiO_2/c-plane GaN capacitors.[4,5]

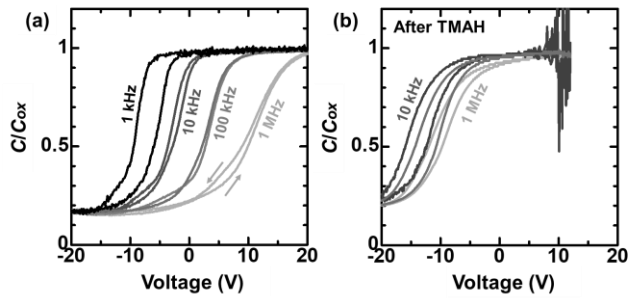

Fig. 3: (a) *C-V* curves of SiO_2/ m-plane GaN MOS capacitors measured under dark condition at room temperature for different frequencies. (b) *C-V* curves of SiO_2/ m-plane GaN MOS capacitors treated by TMAH at 70°C for 30 min.

After dipping TMAH (tetramethyl ammonium hydroxide) solution, which is usually used as the etching process for c-plane GaN trench MOSFETs, the *C-V* curves show the negative shift, as shown in Fig. 3 (b). The MOS structure treated by TMAH increased the interface state density to 3.6×10^{11} cm^{-2}/eV, suggesting that a positive fixed charge increases at the SiO_2/m-plane GaN interface by the TMAH treatment.

Characteristics of m-plane GaN MOSFET

Output characteristics at room temperature for the MOSFET with a m-plane GaN channel parallel to the [0001] direction without the TMAH treatment is shown in Fig. 4 (a). The MOSFETs have a normally-on operation with pinch-off characteristics for V_{gs} < -2.5 V because of the negatively charged UID GaN channel. The subthreshold swing was 1.2 V/decade. I_d is effectively modulated by V_{gs} and shows good saturation. The maximum I_d was 18 mA/mm for V_{gs} = +12 V. The MOSFET with L_{gd} of 6 μm at a drain-voltage (V_{ds}) = +6 V at room temperature is shown in Fig. 4 (b). At room temperature, the off-state I_d was under 1 μA/mm at V_{gs} = –10 V and increased with increasing V_{gs} due to a leakage current through the Mg-doped GaN layers. The I_d on/off ratio was ~10^5.

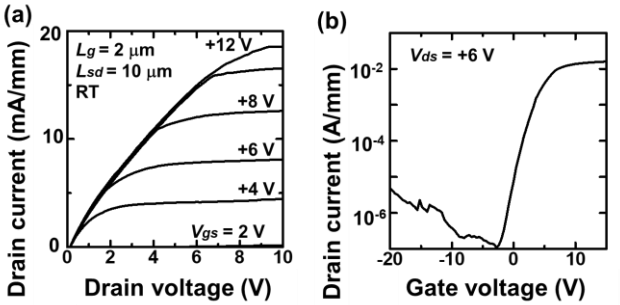

Fig. 4: (a) DC output characteristics of m-plane GaN MOSFET with gate length of 2 μm at room temperature for V_{gs} from 0 to +12 V. (b) Transfer characteristics at a drain voltage of +6 V.

3. Conclusions

We report on the electrical characteristics of m-plane GaN layers. The Si-doped m-plane GaN layer exhibits an ohmic behavior, showing the contact resistance of 2×10^{-5} Ωcm^{-2} and the sheet resistance of 609 Ω/□. Additionally, we achieved the demonstration of the m-plane GaN MOSFETs due to the insertion of Mg-doped GaN back-barrier layer, showing the high transistor on/off ratio of ~10^5.

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