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Preparation and thermoelectric characterization of phosphorus-doped silicon nanocrystals/silicon oxide multilayers

Hisayoshi Kobayashi[1], Ryushiro Akaishi[1], Shinya Kato[2], Masashi Kurosawa[1], Noritaka Usami[1], and Yasuyoshi Kurokawa[1]

[1] Nagoya Univ.
Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan
Phone: +81-52-789-3246 E-mail: kobayashi.hisayoshi@c.mbox.nagoya-u.ac.jp
[2] Nagoya Inst. Tech.
Gokiso-cho, Showa-ku, Nagoya, 466-8555, Japan
Phone: +81-52-735-7966

Abstract

Phosphorous-doped silicon nanocrystals (Si-NCs)/silicon oxide (SiO_y) multilayers were prepared by plasma enhanced chemical vapor deposition (PECVD) and post-annealing. The diameter of Si-NCs were changed by varying the thickness of Si-rich amorphous silicon oxide (a-SiO_x) layer from 3 to 10 nm. Electrical and thermal conductivity of Si-NCs/SiO_y multilayers were decreased with decreasing the diameter (*d*) of Si-NCs. Thermal conductivity at *d*=3 nm was estimated at 1.48 $W \cdot m^{-1} \cdot K^{-1}$, which is much lower than that of bulk Si. These results show that phosphorus doped Si-NCs/SiO_y multilayers are promising for thermoelectric materials.

1. Introduction

Wireless sensor network technology based Internet of things (IoT) is getting important to realize the enhancement of the security and convenience in our society. Conventional batteries in IoT produce environmental concerns and have limited operational life. Harvesting ambient environmental energy is important for sustainable green power used in wireless and portable devices in IoT. Solar cells, electlet, rectenna, thermoelectric devices, and so on are studied as candidates of energy harvesting devices. Silicon is one of abundant materials on the earth and nontoxic. Therefore, there are huge infrastructure and know-how available for its production and processing. It is also possible to combine silicon-based thermoelectric devices with other IoT devices. However, bulk Si is a poor thermoelectric material since it has high thermal conductivity. Many researchers have tried nanostructuring of thermoelectric materials to obtain high Seebeck coefficient and low thermal conductivity [1-3].

In previous research, silicon nanocrystals (Si-NCs)/SiO_y multilayer were prepared by PECVD and post-annealing [4]. The diameter of Si-NCs can be controlled by varying the thickness of Si-rich layer. Therefore, the diameter of Si-NCs can be adjusted below phonon mean free path, leading to the reduction of thermal conductivity. Moreover, as the density of Si-NCs becomes higher in the Si-NC layers, power factor of the Si-NCs layer will approach to that of polycrystalline silicon. Therefore, it is expected that Si-NCs/SiO_y multilayers realize high dimensionless figure of merit (*ZT*). In this study, we prepared phosphorous doped amorphous silicon oxide (a-SiO_x) single layers and stacks of Si-NCs embedded in a-SiO_y as n-type thermoelectrical materials, and evaluated their electrical and thermoelectric properties.

2. Experimental method

Phosphorous-doped a-SiO_x was prepared by PECVD. Setting substrate temperature, pressure, and RF power density were kept at 285 °C, 25 Pa, and 0.0325 W/cm^2, respectively. Both of CO_2 and SiH_4 flow rates were fixed at 10 sccm, and PH_3 flow rate was varied from 1 to 50 sccm. After the deposition, the samples were annealed at 900, 950, and 1000 °C for 30 minutes under forming gas atmosphere (N_2: 97%, H_2: 3%). Silicon oxide multilayers (a-SiO_x:H/a-SiO_y:H) were also prepared by PECVD. The oxygen composition of each layer was set as *x* is less than *y*. It is a purpose that the a-SiO_x and a-SiO_y layer were converted into Si-NCs layer and phonon scattering layer after annealing, respectively. Thickness of a-SiO_x was varied from 3 to 10 nm and that of a-SiO_y was fixed at 2 nm. The flow rates of SiH_4, CO_2 and PH_3 were 10, 10 and 10 sccm for the a-SiO_x layer, and 4, 50 and 0 sccm for the a-SiO_y layer. After the deposition, the samples were annealed at 900, 950, and 1000 °C for 30 minutes under forming gas atmosphere.

Raman scattering spectra were measured to characterize generation of Si-NCs. Spectroscopic ellipsometry (SE) was used to evaluate film thickness with a J. A. Woollam M2000 ellipsometer. Electrical conductivity was measured by *I-V* measurement. Furthermore, thermal conductivity of Si-NCs/SiO_y multilayers was measured by the light pulse

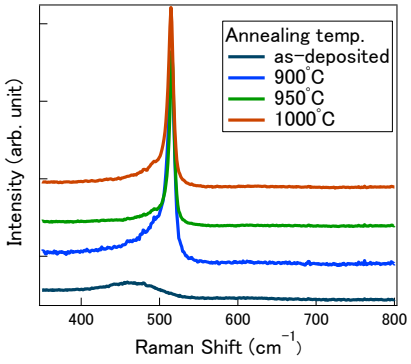

Fig. 1. Raman scattering spectra of the a-SiO_x single layer before and after annealing.

heating thermoreflectance method [5].

3. Results and discussion

Fig. 1 shows the results of Raman scattering spectra of the a-SiO_x single layer before and after annealing. The PH_3 gas flow rate was 10 sccm. No crystalline silicon phase exists in the sample before annealing. The broad peak located at approximately 480 cm^{-1} can be assigned as the transverse optical (TO) phonon mode of an amorphous phase. On the other hand, a sharp peak derived from the crystalline silicon phase can be seen at approximately 510 cm^{-1} after annealing, suggesting the formation of a nanocrystalline silicon phase.

Fig. 2 shows crystal volume fractions evaluated by the ratio of I_c to (I_c+I_a), where I_c and I_a are the intensities of the peaks for the crystalline silicon phase and for the amorphous phase, respectively. The crystal volume fractions were increased with increasing annealing temperature and PH_3 gas flow rate, suggesting that the growth of Si-NCs was enhanced by higher temperature and the impurity nucleation was enhanced by more phosphorus atoms.

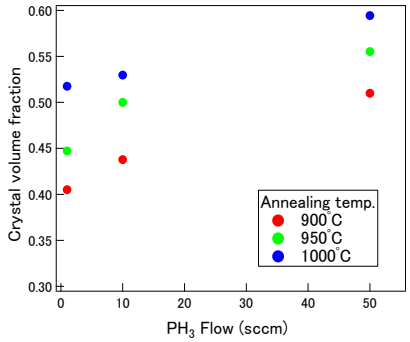

Fig. 2. Crystal volume fraction of the a-SiO_x single layers after annealing as a function of PH_3 flow rate.

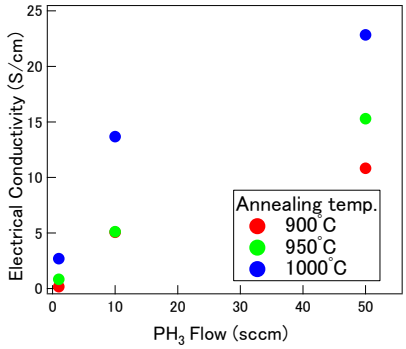

Fig. 3. Electrical conductivity of the a-SiO_x single layers after annealing as a function of PH_3 flow rate.

Fig. 3 shows the electrical conductivity of a-SiO_x single layer. The conductivity was increased with PH_3 gas flow rate. Carrier density was increased by phosphorous doping. Moreover, from the results of Raman scattering spectra, crystal volume fraction was increased with increasing PH_3 gas flow rate and crystallization of Si led to the enhancement of carrier mobility and dopant activation rate. That is why the electrical conductivity was increased.

Fig. 4 shows the results of electrical and thermal conductivity for Si-NCs/SiO_y multilayers (Si-NC diameter: d=3, 5, 10 nm). The results clearly show the trend that as the grain size of Si-NCs were smaller, the electrical and thermal conductivity were lower. The decrease of electrical conductivity was derived from the decrease of crystal volume. On the other hand, since the phonon with short mean free path was strongly scattered at the Si-NCs/SiO_y interface and grain boundary, the thermal conductivity was much smaller than that of polycrystalline silicon (149 $W \cdot m^{-1} \cdot K^{-1}$ [6]), suggesting that nanostructuring of silicon can reduce the thermal conductivity drastically.

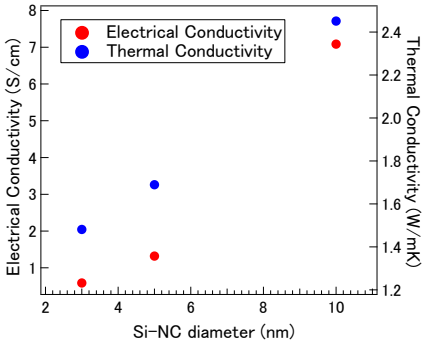

Fig. 4. Electrical and thermal conductivity of the Si-NCs/SiO_y multilayers as a function of the Si-NC diameter.

4. Conclusions

Phosphorus-doped silicon oxide multilayers (a-SiO_x:H/a-SiO_y:H) were prepared by PECVD. The oxygen composition of each layer was set as x is less than y. It is a purpose that the a-SiO_x and a-SiO_y layer were converted into Si-NCs layer and phonon scattering layer after annealing at 900-1000 °C, respectively. The diameter of Si-NCs were changed by varying the thickness of Si-rich a-SiO_x layer from 3 to 10 nm. Electrical and thermal conductivity of Si-NCs/SiO_y multilayers were decreased with decreasing the diameter (d) of Si-NCs. Thermal conductivity at d=3 nm was estimated at 1.48 $W \cdot m^{-1} \cdot K^{-1}$, which is much lower than bulk Si. These results show that phosphorus doped Si-NCs/SiO_y multilayers are promising for thermoelectric materials.

Acknowledgements

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References

[1] Y. Nakamura, M. Isogawa, T. Ueda, S. Yamasaka, H. Matsui, J. Kikkawa, S. Ikeuchi, T. Oyake, T. Hori, J. Shiomi, A. Sakai, Nano Energy **12** (2015) 845.

[2] M. Nomura, J. Nakagawa, Y. Kage, J. Maire, D. Moser, O. Paul, Appl. Phys. Lett. **106** (2015) 143102.

[3] Z. Wang, J. E. Alaniz, W. Jang, J. E. Garay, C. Dames, Nano Lett. **11** (2011) 2206.

[4] Y. Kurokawa, S. Yamada, S. Miyajima, A.Yamada, and M. Konagai, Curr. Appl. Phys. **10** (2010) S435.

[5] T. Baba, *1*st *International Symposium on Thermal Design and Thermophysical Property for Electronics,* June 18-20, 2008, Tsukuba.

[6] C. Y. Ho, R. W. Powell, and P. E. Liley, J. Phys. Ref. Data **1** (1972) 279.