Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp1037-1038

A 17.6-to-24.3 GHz -193.3-dB FoM$_T$ LC-VCO for 60-GHz Wireless Applications

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Abstract

This paper presents a 20-GHz low-phase-noise low-power LC-VCO for 60-GHz wireless applications. It adopts a fully differential tuning varactor, a coarse and a fine capacitor array to cover wide tuning range with small tuning gain to reduce the amplitude-to-phase noise conversion. A novel layout floorplan is proposed to reduce the impact of the parasitic resistance of the interconnect and thus improve the Q of the LC tank in the VCO. Hence, the phase noise can be reduced without increasing power consumption. Implemented in 65-nm CMOS process, the prototype achieves 17.6-24.3-GHz frequency range, -124-dBc/Hz@10MHz phase noise at 20.1-GHz carrier frequency, 4.9-mW DC power, and -193.3-dB figure-of-merit (FOM$_T$).

1. Introduction

The 20-GHz phase-locked loop (PLL) [1] has become popular for the 60-GHz wireless applications such as IEEE 802.11ay [2]. The 20-GHz LC voltage-controlled oscillator (LC-VCO), which dictates the out-band phase noise of the 20-GHz PLL [1], is the critical building block. In the previous 20-GHz LC-VCOs [3-5], although the multi-bit capacitor array is adopted to cover wide frequency range, a relative large VCO tuning gain (>1 GHz/V) is still required to avoid blind zone, which results in poor phase noise due to the amplitude-to-phase noise (AM-PM) conversion [6]. What's more, the parasitic resistance of the multi-bit capacitor array [3-5] significantly degrades Q of the LC-tank at frequency higher than 20 GHz. This results in high power consumption and degraded phase noise.

In this paper, we propose a 20-GHz low-phase-noise low-power LC-VCO for 60-GHz wireless applications. It adopts a fully differential tuning varactor and two digitally-controlled capacitor arrays (DCCA) to cover wide tuning range with small tuning gain to reduce the AM-PM noise conversion. A new layout floorplan scheme is proposed to reduce the impact of the parasitic resistance of the interconnect and thus improve the Q of the LC tank. So, the phase noise is reduced without increasing power consumption.

2. Circuit Design

Figure 1 presents the schematic of the proposed 20-GHz LC-VCO. The VCO adopts the NMOS-only structure instead of the PMOS-only structure or CMOS structure to reduce the parasitic and guarantee wide tuning range. Small tuning gain is necessary to reduce the level of the AM-PM

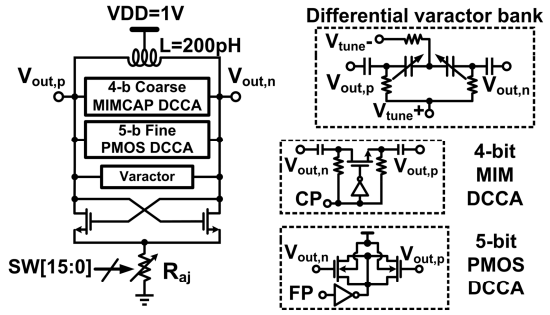

Fig. 1. Schematic of the proposed 20GHz LC-VCO.

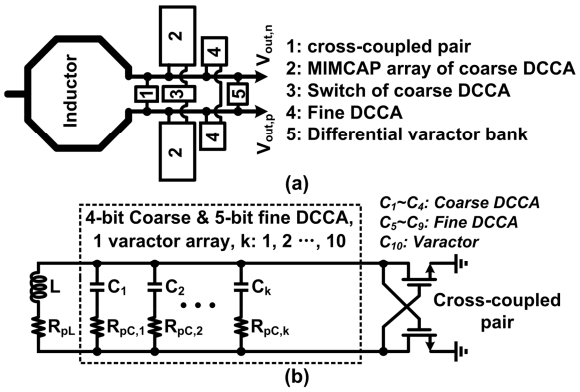

Fig. 2. (a) Proposed layout floorplan. (b) Equivalent circuit of the LC-VCO for calculation the equivalent quality factor.

noise conversion and thus improve the phase noise performance. In this design the fully differential tuning structure is adopted to widen the tuning range with small tuning gain. Post-layout simulation shows the tuning gain is about 70~100 MHz/V over all covered frequency range, which is much lower than that in [3-5]. What's more, fully differential tuning structure has better PSRR performance than single-ended counterpart. Since the VCO tuning gain is low, a 4-bit coarse metal-isolator-metal (MIM) capacitor based DCCA and a 5-bit fine PMOS capacitor based DCCA are adopted to achieve wide tuning range without blind zone. A 16-bit adjustable tail resistor array (R_{adj}) is used to prevent the loss induced by the NMOS transistor while avoid the flicker noise up-conversion of the current source.

3. Layout Design

Figure 2(a) shows the proposed layout floorplan scheme. The inductor and the coarse DCCA are placed as close to the cross-coupled pair as possible to reduce the impact of parasitic resistance of the LC-tank. Thus, the Q of the LC-tank is improved and the VCO phase noise is reduced without in-

creasing power consumption. The reason is as follows.

Figure 2(b) shows the equivalent circuit of the LC-VCO. L is the tank inductance. R_{pL} is the equivalent parasitic resistance of interconnect between the inductor and the NMOS pair. Since there are several capacitors in the coarse/fine DCCA and varactor array, we use C_k to express the capacitance of each capacitor in the VCO, as shown in Fig. 2(b). The parasitic capacitor is also taken into account in C_k. $R_{pC,k}$ is the equivalent parasitic resistance of the interconnect between the capacitor C_k and the NMOS pair. The equivalent quality factor of the inductor, the capacitor C_k, and the total LC tank, can be respectively written as

$$Q_{eqL} = \omega L / (\frac{\omega L}{Q_L} + R_{pL}) \quad (1)$$

$$Q_{eqC,k} = 1/(\omega C_k (\frac{1}{\omega C_k Q_{C,k}} + R_{pC,k})) \quad (2)$$

$$Q_{eqTank} = (\frac{1}{Q_{eqL}} + \frac{1}{Q_{eqC,1}} + \frac{1}{Q_{eqC,2}} + \cdots + \frac{1}{Q_{eqC,k}})^{-1} \quad (3)$$

where Q_L and $Q_{C,k}$ is the quality factor of the inductor and the capacitor C_k without the influence of the interconnect, respectively. As indicated in (1), the inductor needs to be as close to the cross-coupled pair as possible to reduce R_{pL} and thus increase Q_{eqL}. As equation (2) shows, with same $R_{pC,k}$, large C_k causes more $Q_{eqC,k}$ degrading than small C_k. So, the large capacitors should be nearer to the cross-coupled pair than the small capacitors to reduce $Q_{eqC,k}$ degrading induced by $R_{pC,k}$, and thus it is necessary to put the coarse DCCA nearer to the NMOS pair than the fine DCCA and differential varactor array, as shown in Fig. 2(a). As indicated in (3), Q_{eqTank} is improved with the improvement of Q_{eqL} and $Q_{eqC,k}$. Hence, using the proposed layout floorplan scheme can achieve an improved Q of LC tank.

4. Implementation and Measurement Results

The proposed LC-VCO is implemented in 65 nm CMOS and the core area is 0.29×0.215 mm^2 exclude the output buffer for testing purpose, as shown in Fig. 3. Fig. 3 also shows the measured frequency tuning range (FTR) is from 17.6 GHz to 24.3 GHz (32%). Fig. 4 presents the measured phase noise at 20.1-GHz output. The phase noise is -124 dBc/Hz@10MHz. The phase noise at 1-MHz and 10-MHz offset frequency over covered frequency range is presented in Fig 5. The measured power consumption is 4.9 mW. This work achieves wider FTR, lower power consumption, and better figure-of-merit (FOM and FOM$_T$), compared with other recently published works listed in Table I.

5. Conclusions

This paper presented a 20-GHz low-phase-noise low-power LC-VCO for 60-GHz wireless applications with a novel layout floorplan scheme. Measurement results show a FTR of 17.6-to-24.3 GHz, 4.9-mW power consumption, -124 dBc/Hz@10MHz and -193.3-dB FOM$_T$.

Acknowledgements

This work was supported by the National Key R&D Program of China (Grant No. 2016YFA0202200), Youth Innovation Promotion Association Program, Chinese Academy of Sciences (No. 2016107), National Natural Science Foundation of China (No. 61874107), and Beijing Municipal Science and Technology Project (No. Z181100008918009).

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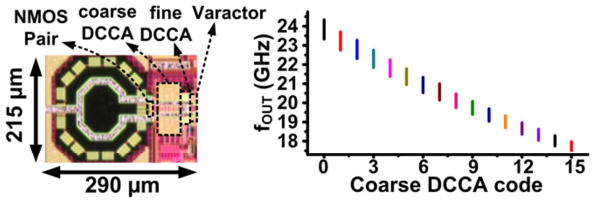

Fig. 3. Chip micrograph and measured frequency tuning range.

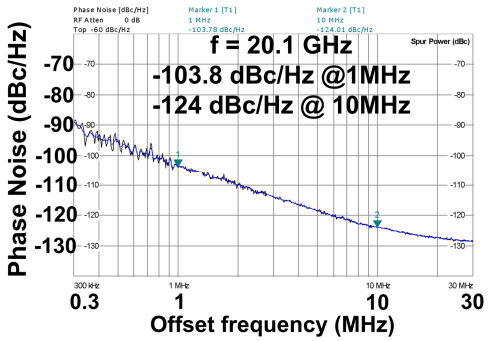

Fig. 4. Measured phase noise at carrier frequency of 20.1 GHz.

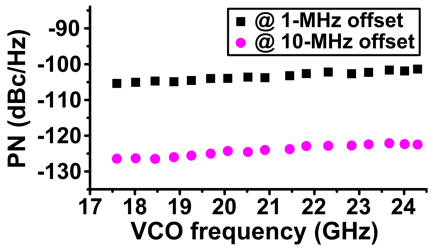

Fig. 5. Phase noise over covered frequency range.

Table I. Performance summary and comparison

	This work	[3]	[4]	[5]
Process	**65 nm**	65 nm	90 nm	32 nm
FTR (GHz)	**17.6~24.3**	NA	24.1~28.2	21.8~27.5
FTR (%)	**32**	15.8	16	23
PN (dBc/Hz)	**-103.8 @ 1 MHz -124 @ 10MHz (20.1 GHz)**	-100.7 @1MHz (20.85 GHz)	-101.2 @1MHz (25.5 GHz)	-127.3 @10MHz (24.7 GHz)
Power (mW)	**4.9**	8.1	11	24
Supply (V)	**1**	NA	1.2	0.7~1.5
FOM (dBc/Hz)[A]	**-183.2 @ 10 MHz**	-177.8 @ 1 MHz	-178.9 @ 1 MHz	-181.3 @ 10 MHz
FOM$_T$ (dBc/Hz)[B]	**-193.3 @ 10 MHz**	-181.8 @ 1 MHz	-183 @ 1 MHz	-188.6 @ 10 MHz

[A]FOM= PN-20log(f_0/Δf)+10log(P_{DC}/1mW), the lower the better
[B]FOM$_T$=FOM-20log(FTR/10), the lower the better