Extended Abstracts of the 2019 International Conference on Solid State Devices and Materials, Nagoya, 2019, pp1041-1042

A Fast-Locking All-Digital PLL with Dynamic Loop Gain Control and Phase Self-Alignment Mechanism for Sub-GHz IoT Applications

Hsi-Hua Wang[1], Yu-Lung Lo[1*], and Wei-Bin Yang[2]

[1] Department of Electronic Engineering, National Kaohsiung Normal University, Kaohsiung City, Taiwan
[2]Department of Electrical Engineering, Tamkang University, New Taipei City, Taiwan
Phone: +886-7-7172930#7917 *Email: yllo@nknu.edu.tw

Abstract

This paper describes a fast-locking all-digital PLL (ADPLL) with dynamic loop gain control and phase self-alignment mechanism. Compared with the conventional fast-locking ADPLLs, this paper proposes the phase self-alignment mechanism to solve the over-damping caused by the large K_I. Therefore, the proposed ADPLL can not only reduce the locking time but also maintain the jitter performance. Based on a 0.18-µm standard CMOS process with a supply voltage of 1.8 V, the experimental results indicated that the proposed ADPLL can reduce 91% of the locking time. The output frequency range of the proposed ADPLL is 0.7–1 GHz that can be suitable for sub-GHz IoT band applications. At 700 MHz, the power consumption is 8.25 mW, peak-to-peak jitter is 22.3 ps, and core area is 0.291 mm^2.

1. Introduction

In recent years, phase-locked loop (PLL) has been widely used in various communication systems and radio fields, such as Bluetooth, WIFI, Internet of Things (IoT), GSM, GPS, etc. [1] [2]. Compared with analog PLL, the ADPLL has smaller area, faster locking speed and good stability to process, voltage, and temperature (PVT) drift [3] [4]. With the advent of the 5G generation, the application of the IoT is growing at an astonishing speed insofar as, it is projected 50 billion IoT devices by the end of 2020 [3]. In the IoT systems, the transmitter and receiver must raise the fundamental signal to a specified frequency band or reduce the received signal to the fundamental frequency. Since different devices need to transmit different carrier frequencies, PLLs with high accuracy, high stability, fast switching speed, and low power is needed. Therefore, a fast-locking all-digital PLL proposed in this paper not only has faster switching speed but also can effectively reduce the power consumption while the loop tracking.

2. Proposed Fast-Locking ADPLL

The proposed ADPLL in this paper consists of a phase frequency detector (PFD), a time-to-digital converter (TDC), a digital loop filter (DLF), a digitally controlled oscillator (DCO), and a resettable frequency divider (RFD), as shown in Fig. 1. The working stage of ADPLL is divided into three stages. The first is the detecting stage. The RST signal is inputted at the beginning of the detecting stage to reset the ADPLL and align the feedback frequency (F_{BK}) with the reference frequency (F_{REF}) through the phase self-alignment mechanism by the DLF with lock detector (LD) and counter, and RFD. Then the PFD compares the frequency between F_{REF} and F_{BK}. The second stage is the setup stage. At this stage, which bands of DCO should be used is according to the value of the previous stage. The MSB code of DCO is set to high, and the others are set to low. By this, DCO can track from the middle of DCO frequency band to reduce the unnecessary lock time. The third stage is the tracking stage. The ADPLL will start tracking at this time. In order to achieve fast-locking, the dynamic loop gain control mechanism is proposed to improve tracking speed by using a larger K_I in DLF. However, a large K_I will lead to a decrease in the stability of the system, and will also make over-damping of the circuit during tracking, which may cause an increase in the tracking time [5]. Hence, a phase self-alignment mechanism is proposed, which is consists of LD and counter in DLF, and RFD. When the output frequency is close to the target frequency, the LD will be high. At this moment, the RFD is reset by the RST pulse signal and the value of K_I is changed to small one. Therefore, the phase of F_{BK} can be aligned with F_{REF} to reduce the extra tracking time caused by over-damping. When the loop locked, the value of K_I will become smaller to maintain loop stability and jitter performance. The flowchart and the waveform diagram of the proposed ADPLL, as shown in Fig. 2.

3. Experimental Results

Fig. 3 shows the layout of the proposed ADPLL and the core area is 0.291 mm^2. Fig. 4 shows the locking results of the proposed ADPLL and the proposed ADPLL without phase self-alignment mechanism, and the conventional ADPLL. Compared with conventional ADPLL and the proposed ADPLL without phase self-alignment mechanism, the lock time can be reduced by 91% and 83%, respectively. The locking time of the ADPLL locked at 700MHz and 1GHz, as shown in Fig. 5. The jitter of ADPLL at 700MHz is 22.3 ps which is 1.56% of the output period, as shown in Fig. 6. Table I shows a comparison of the performances of recently fast-locking ADPLLs. Finally, the proposed ADPLL with dynamic loop gain control and phase self-alignment mechanism has less locking time and lower power consumption.

4. Conclusions

A fast-locking all-digital PLL with dynamic loop gain control and phase self-alignment mechanism is proposed in this paper. In this paper, a phase self-alignment mechanism is proposed to solve the problem of over-damping by large K_I and reduce the locking time of ADPLL. Compared with the conventional ADPLL, the proposed fast-locking ADPLL can reduce the locking time from 144 cycle to 13 cycle which is reduced the locking time of 91%. The proposed ADPLL exhibited superior performance with the locking time, power, and jitter, and is suitable for sub-GHz IoT band applications.

References

[1] Y. He, et al., "A 673μW 1.8-to-2.5GHz dividerless fractional-N digital PLL with an inherent frequency-capture capability and a phase-dithering spur mitigation for IoT applications," *ISSCC* (2017) 420–421.

[2] L. –L. Xie, et al., "A portable wide-range all-digital phase-locked loop with fast settling time in 180 nm CMOS," *ICSICT* (2016) 545–547.

[3] J. Gorji, et al., "A process-independent and highly linear DCO for crowded heterogeneous IoT Devices in 65-nm CMOS," *IEEE TVLSI* **25** (2017) 3369–3379.

[4] H. –C. Chu, et al., "A fast-locking all-digital phased-locked loop with a 1 ps resolution time-to-digital converter using calibrated time amplifier and interpolation digitally-controlled-oscillator," *EDSSC* (2016) 375–378.

[5] J. –M. Lin, et al., "A fast-locking all-digital phase-locked loop with dynamic loop bandwidth adjustment," *IEEE TCAS-I* **62** (2015) 2411–2422.

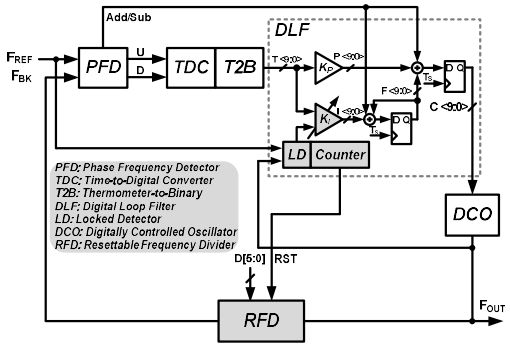
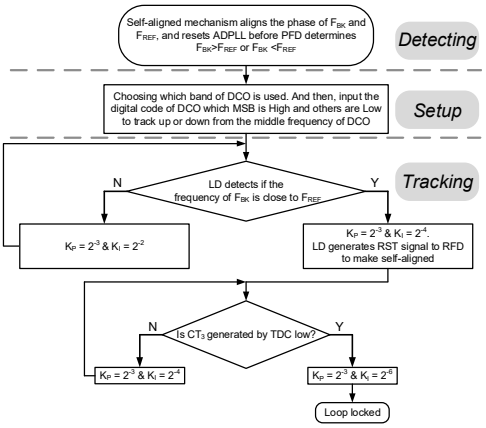
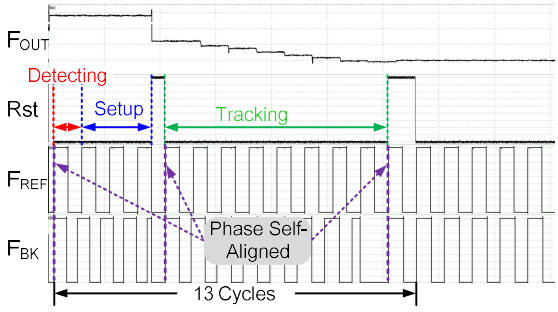


Fig. 1 The architecture of proposed ADPLL.



(a)



(b)

Fig. 2 (a) The flowchart and (b) waveform diagram of the proposed ADPLL.

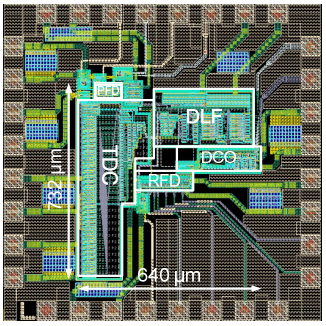


Fig. 3 Layout of proposed ADPLL.

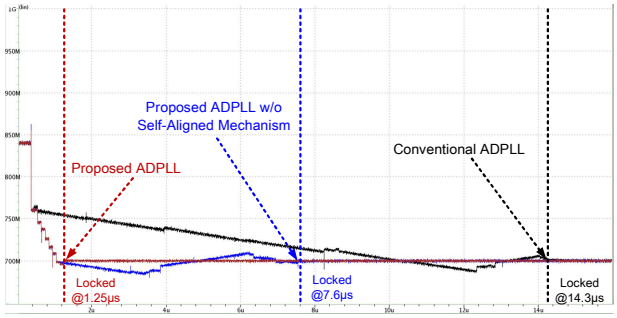


Fig. 4 Comparison of locking time for various ADPLLs.

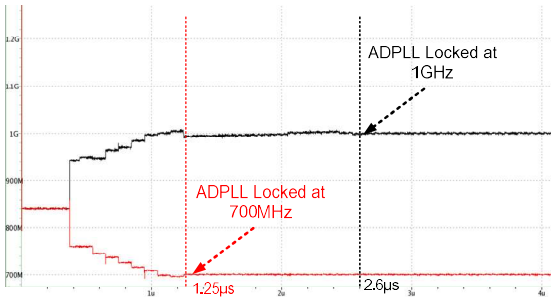


Fig. 5 The locking time of the ADPLL locked at 700MHz and 1GHz.

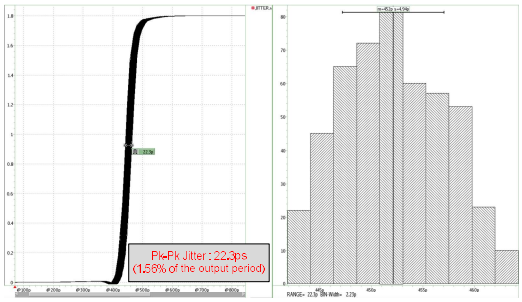


Fig. 6 The jitter of ADPLL and spectrum which locked at 700MHz.

Table I Performance comparison of ADPLLs

Parameters	REF [2]	REF [4]	REF [5]	**This Work**
Process (μm)	0.18	0.18	0.18	**0.18**
Voltage (V)	1.8	1.8	1.8	**1.8**
Freq. Range (GHz)	0.294~ 0.73	0.149~ 1.45	0.2539~ 1.367	**0.7~ 1**
Locking Time	150 cycles @730 MHz	7.52 μs @800 MHz	57 cycles @1.25 GHz	**1.25 μs (13 cycles) @700 MHz**
Area (mm^2)	0.9	0.225	0.7735	**0.291**
P2P Jitter (ps)	N/A	21.9 (1.752%)	32.5 (4.06%)	**22.3 (1.56%)**
Power (mW)	15 @730 MHz	18.2 @800 MHz	35 @1.25 GHz	**8.25 @700 MHz**